

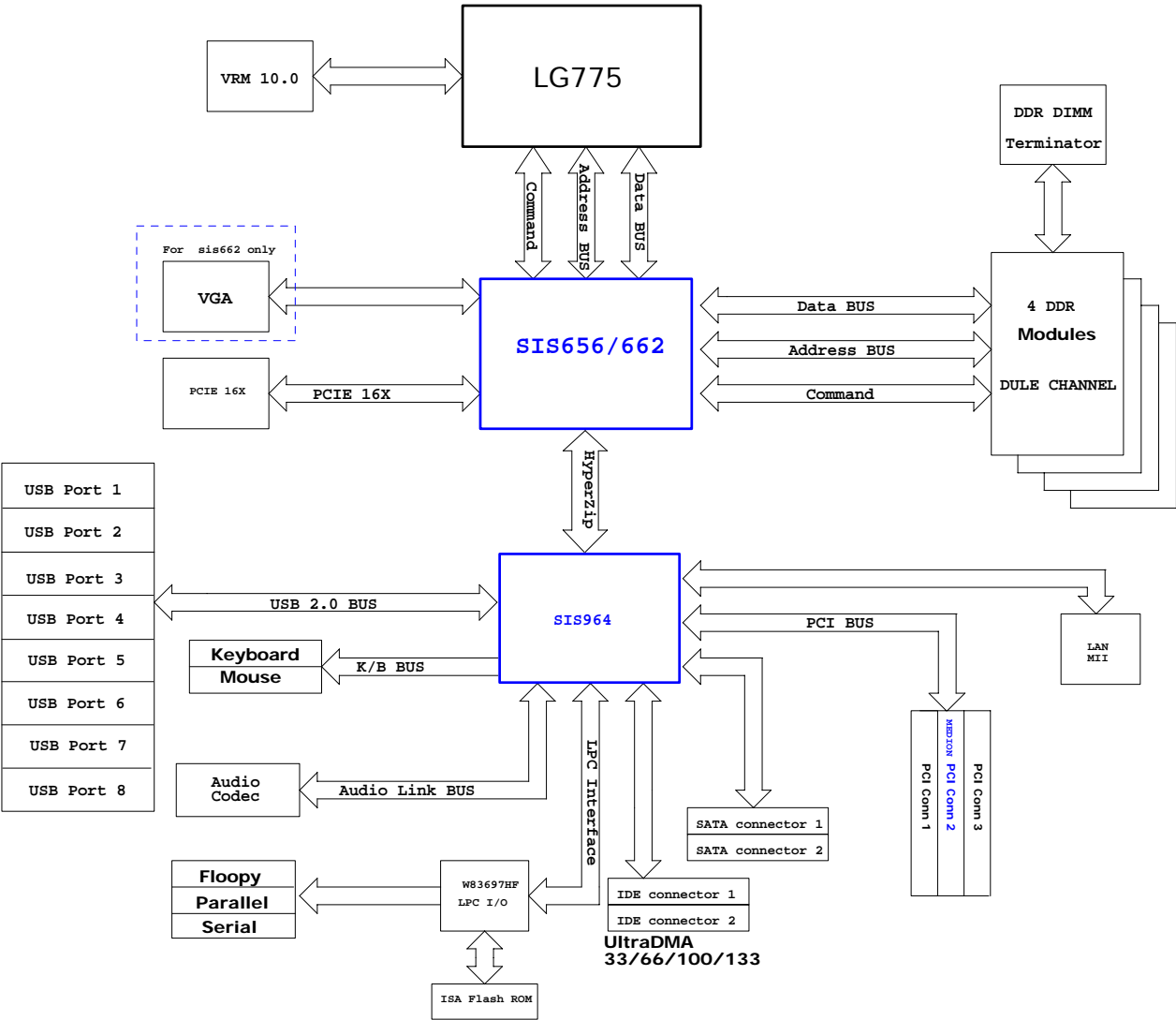
MS-7114 VER:0B uATX

- * *Intel LGA775 Processor*
- * *SIS 656 / 662 + 964*
- * *ICS953401+ICS9P932*
- * *Winbond 83697HF I/O*
- * *LAN-VT6103*
- * *USB 2.0 support x 8*
- * *ALC 850 AC97 CODEC*
- * *IEEE1394-VT6307*
- * *Slot:*
 - DDR DIMM Slot *4*
 - PCI EXPRESS x16 Slot *1*
 - PCI2.2 Slot *3*

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Intel LGA775	4-6
NB SIS 656/662	7-11
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Block Diagram

MS-7114 Ver:0A

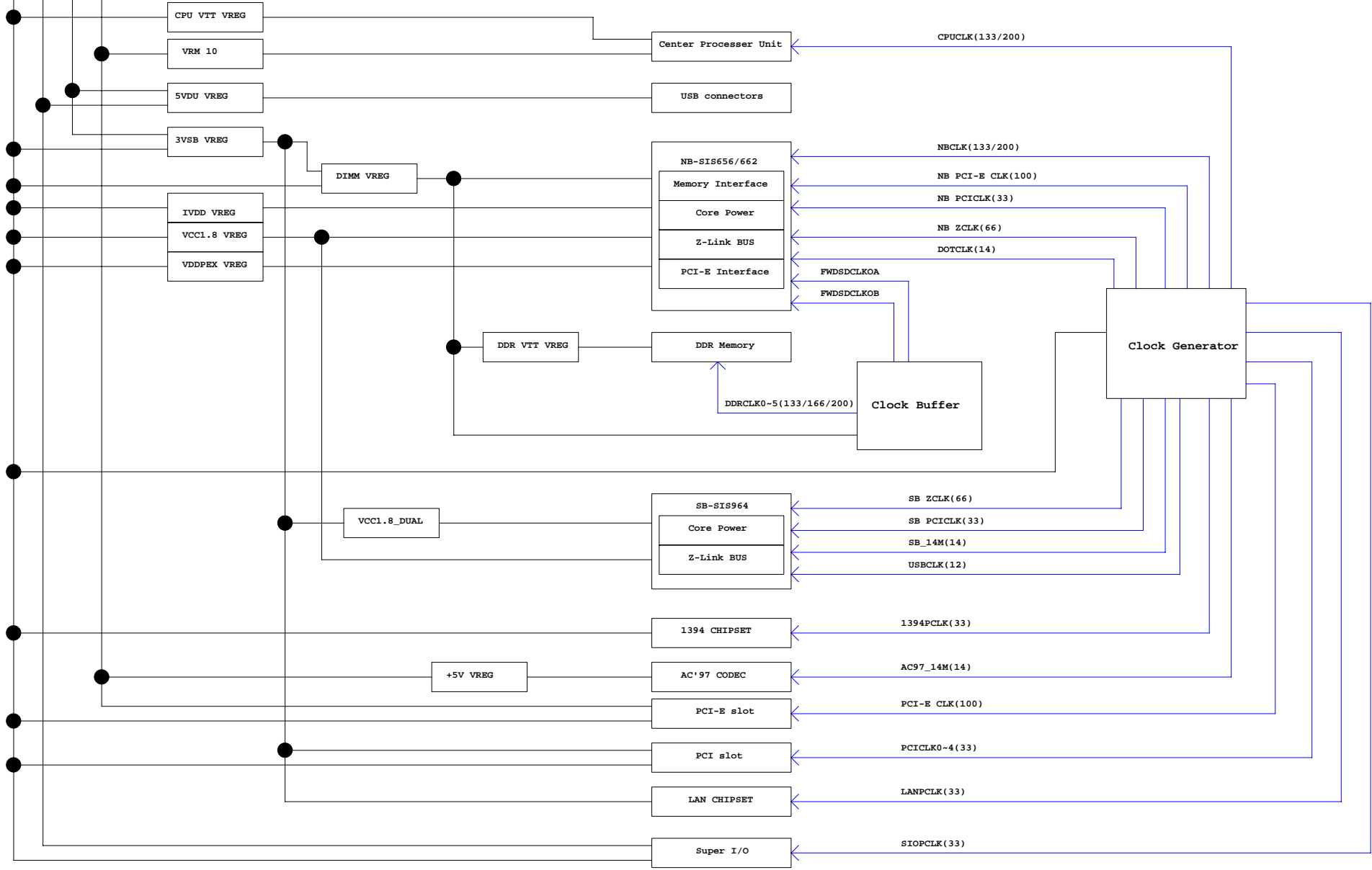


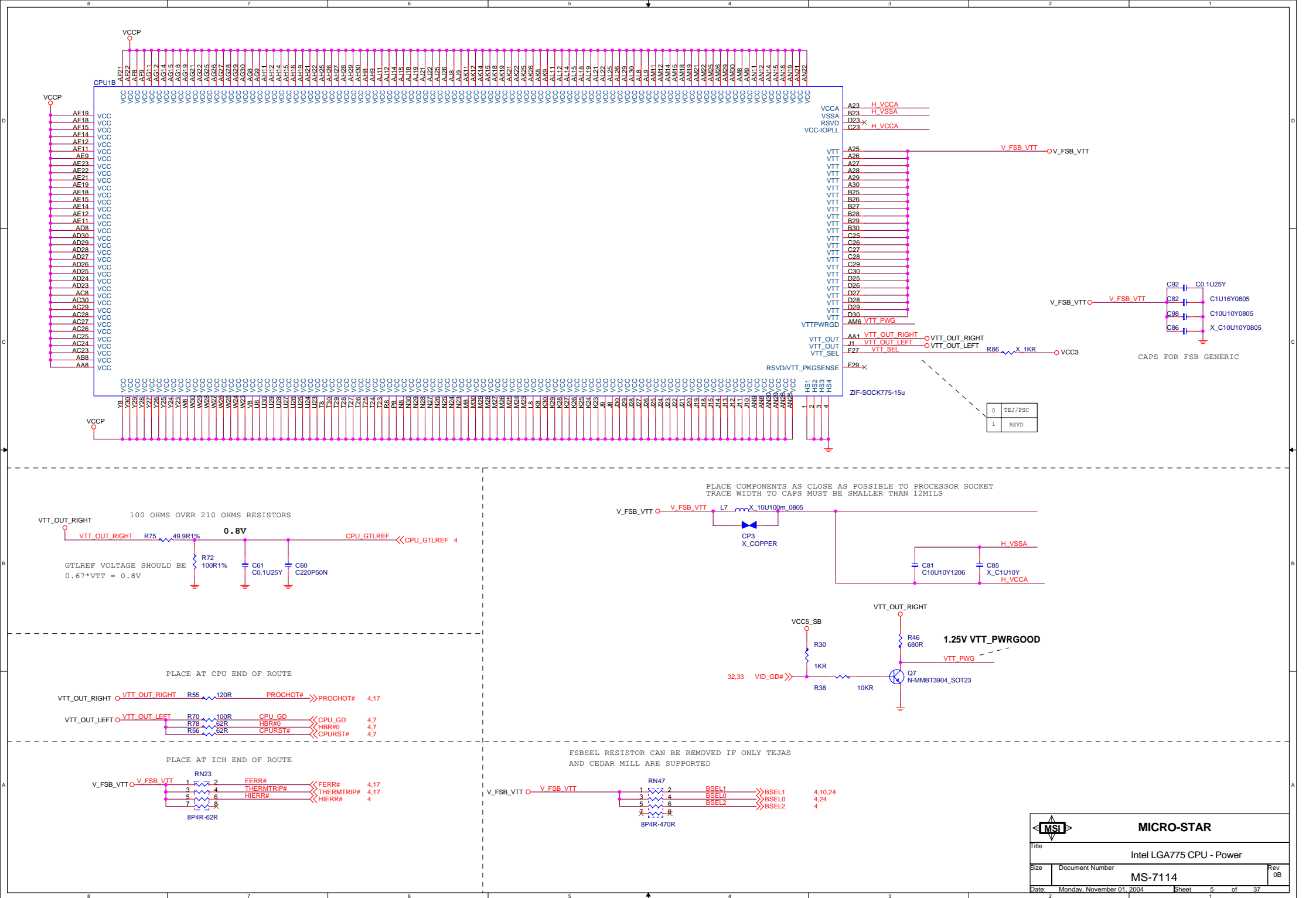
Power Delivery Map

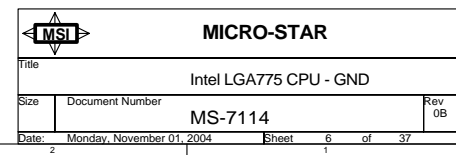
CLOCK Delivery Map

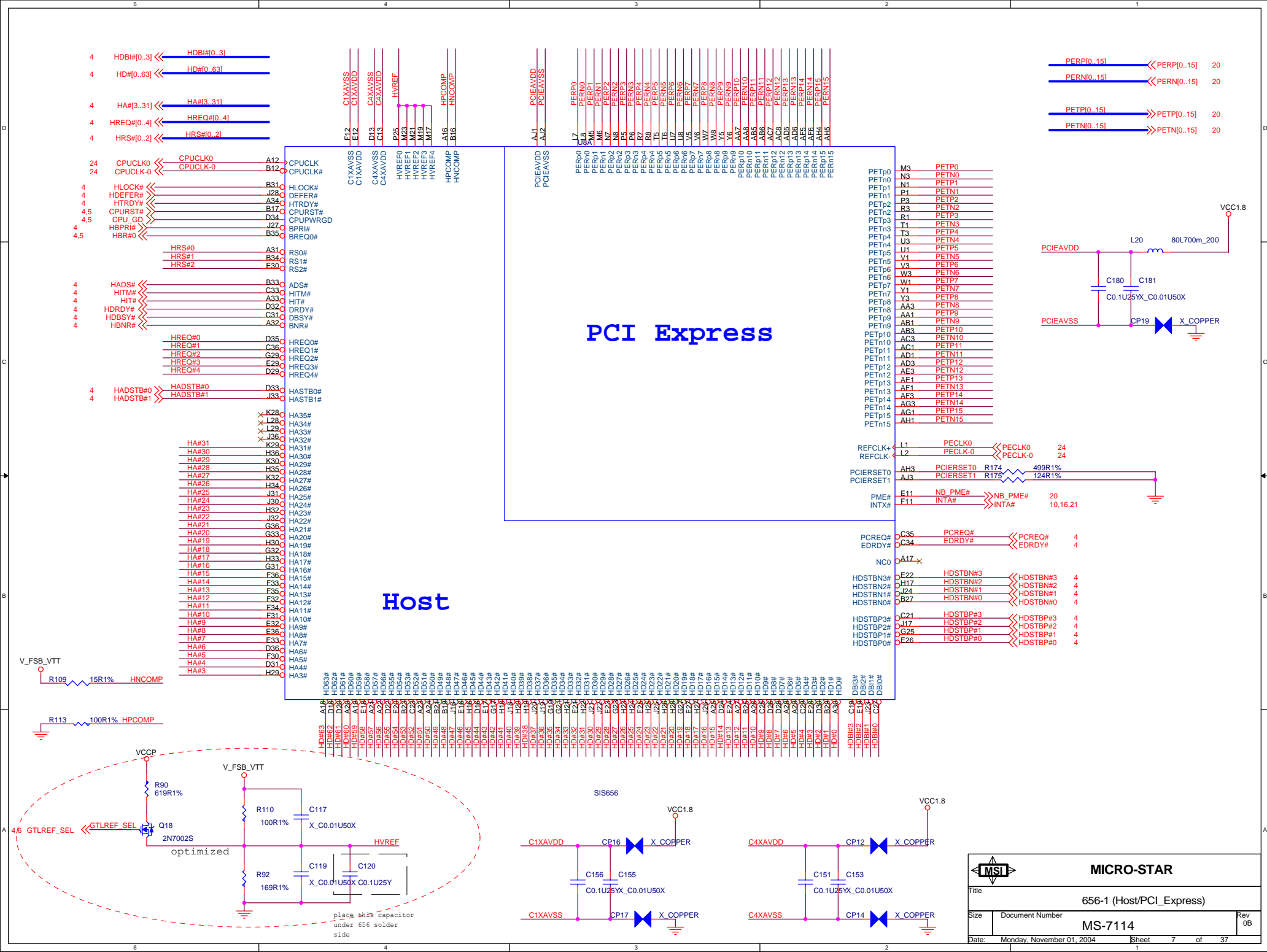
ATX 12V POWER Supply

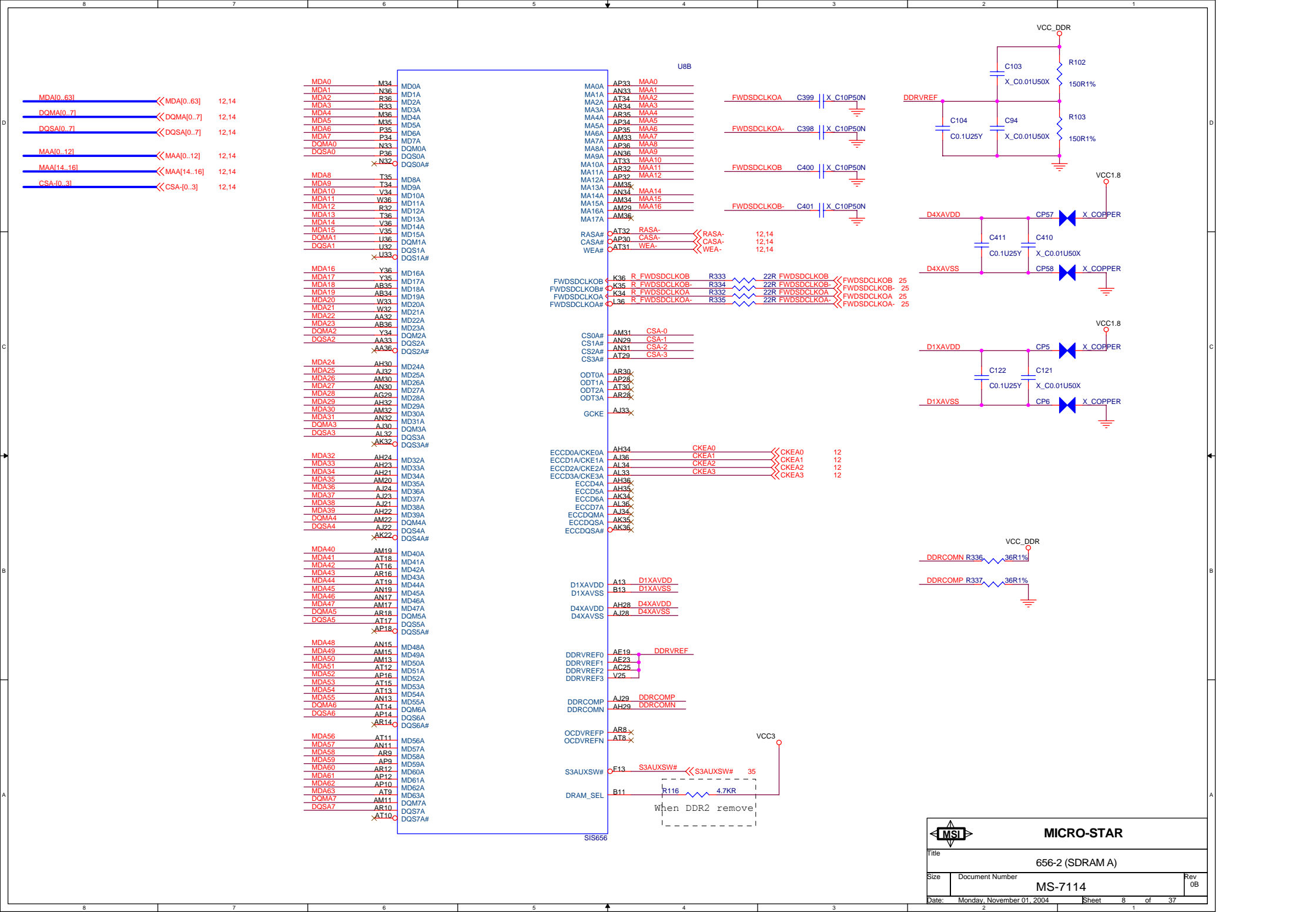
3.3V	5V	5VSB 1A	12V
------	----	------------	-----











MDB[0..63] << MDB[0..63] 13,15
DQMB[0..7] << DQMB[0..7] 13,15
DQS[0..7] << DQS[0..7] 13,15
MAB[14..16] << MAB[14..16] 13,15
MAB[0..12] << MAB[0..12] 13,15
CSB-[0..3] << CSB-[0..3] 13,15

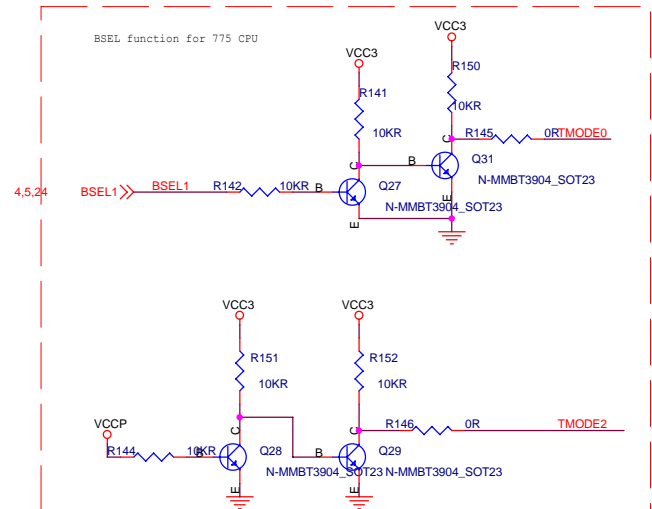
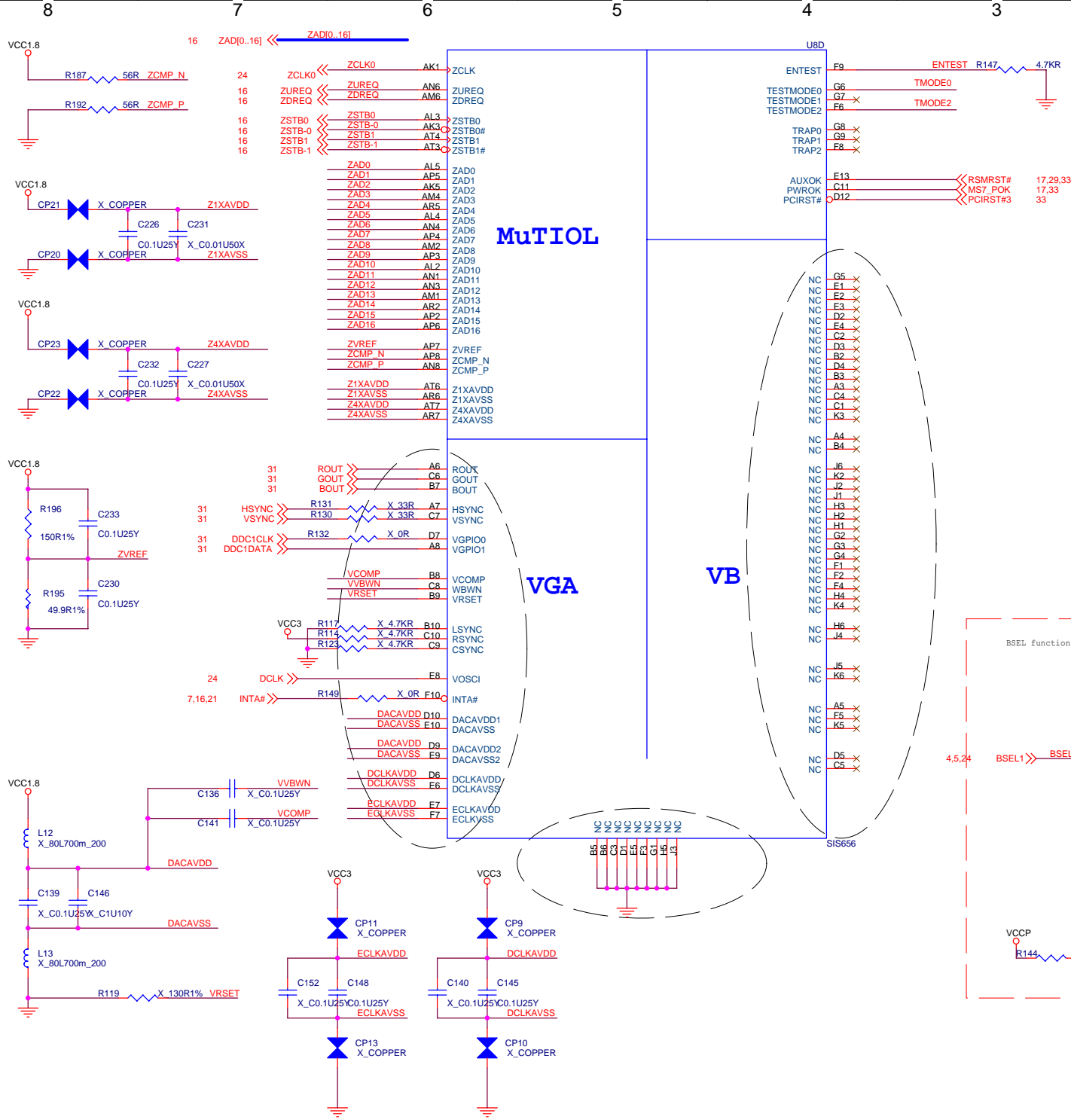
MDB0 N29 MD0B
MDB1 M28 MD1B
MDB2 P28 MD2B
MDB3 R28 MD3B
MDB4 M30 MD4B
MDB5 M29 MD5B
MDB6 P29 MD6B
MDB7 R29 MD7B
DQMB0 N28 DQM0B
DQS0 P30 DQS0B
P32 QDS0B#
MDB8 T29 MD8B
MDB9 U29 MD9B
MDB10 W29 MD10B
MDB11 V28 MD11B
MDB12 T32 MD12B
MDB13 T30 MD13B
MDB14 V30 MD14B
MDB15 V29 MD15B
DQMB1 T28 DQM1B
DQS1 V32 DQS1B
U28 QDS1B#
MDB16 Y30 MD16B
MDB17 Y29 MD17B
MDB18 AB29 MD18B
MDB19 AC29 MD19B
MDB20 W28 MD20B
MDB21 Y32 MD21B
MDB22 AB32 MD22B
MDB23 AB30 MD23B
DQMB2 AA29 DQM2B
DQS2 AA28 DQS2B
Y28 QDS2B#
MDB24 AD32 MD24B
MDB25 AD30 MD25B
MDB26 AE30 MD26B
MDB27 AE29 MD27B
MDB28 AS28 MD28B
MDB29 AC28 MD29B
MDB30 AE28 MD30B
MDB31 AF32 MD31B
DQMB3 AD29 DQM3B
DQS3 AD28 DQS3B
AE29 QDS3B#
MDB32 AJ27 MD32B
MDB33 AM26 MD33B
MDB34 AM24 MD34B
MDB35 AK24 MD35B
MDB36 AM28 MD36B
MDB37 AK28 MD37B
MDB38 AH26 MD38B
MDB39 AH25 MD39B
DQMB4 AK26 DQM4B
DQS4 AJ25 DQS4B
AJ28 QDS4B#
MDB40 AJ19 MD40B
MDB41 AH20 MD41B
MDB42 AH18 MD42B
MDB43 AK20 MD43B
MDB44 AJ20 MD44B
MDB46 AJ18 MD46B
MDB47 AJ17 MD47B
DQMB5 AH19 DQM5B
DQS5 AK18 DQS5B
AJ28 QDS5B#
MDB48 AJ16 MD48B
MDB49 AJ15 MD49B
MDB50 AJ13 MD50B
MDB51 AH14 MD51B
MDB52 AM16 MD52B
MDB53 AK16 MD53B
MDB54 AK14 MD54B
MDB55 AJ14 MD55B
DQMB6 AH16 DQM6B
DQS6 AM14 DQS6B
AJ28 QDS6B#
MDB56 AK12 MD56B
MDB57 AJ12 MD57B
MDB58 AN9 MD58B
MDB59 AM9 MD59B
MDB60 AH13 MD60B
MDB61 AM12 MD61B
MDB62 AM10 MD62B
MDB63 AK10 MD63B
DQMB7 AJ11 DQM7B
DQS7 AH11 DQS7B
AJ28 QDS7B#

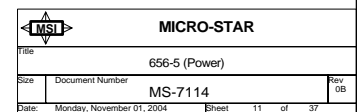
U8C
MA0B AT25 MAB0
MA1B AN25 MAB1
MA2B AM25 MAB2
MA3B AT26 MAB3
MA4B AP26 MAB4
MA5B AT27 MAB5
MA6B AM27 MAB6
MA7B AN27 MAB7
MA8B AG32 MAB8
MA9B AP24 MAB9
MA10B AT24 MAB10
MA11B AR24 MAB11
MA12B AG36 MAB12
MA13B AT28 MAB13
MA14B AG33 MAB14
MA15B AN21 MAB15
MA16B AE34 MAB16
MA17B
RASB# AT23 RASB- << RASB- 13,15
CASB# AR22 CASB- << CASB- 13,15
WEB# AT22 WEB- << WEB- 13,15
ECCD0B/CKE0B AC32 CKEB0 << CKEB0 13
ECCD1B/CKE1B AD36 CKEB1 << CKEB1 13
ECCD2B/CKE2B AF36 CKEB2 << CKEB2 13
ECCD3B/CKE3B AF35 CKEB3 << CKEB3 13
ECCD4B AC33
ECCD5B AE33
ECCD6B AE32
ECCD7B AD33
ECCDQMB AE36
ECCDQSB AD34
ECCDQSB#
CS0B# AN23 CSB-0
CS1B# AM21 CSB-1
CS2B# AM23 CSB-2
CS3B# AT20 CSB-3
ODT0B AP22
ODT1B AR20
ODT2B AT21
ODT3B AP20



MICRO-STAR

Title			656-2 (SDRAM B)
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		1	Rev 0B





25 DDRCLKA[0..5] << DDRCLKA[0..5]
25 DDRCLKA[0..5] << DDRCLKA[0..5]
8,14 MDA[0..63] >> MDA[0..63]
8,14 MAA[0..12] >> MAA[0..12]
8,14 MAA[14..16] >> MAA[14..16]
8,14 DQMA[0..7] >> DQMA[0..7]
8,14 DQSA[0..7] >> DQSA[0..7]

NOTE:

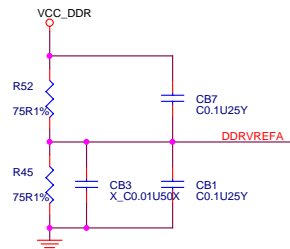
VDDID IS A TRAP ON THE DIMM
MODULE TO INDICATE:

VDDID	REQUIRED POWER
OPEN	VDD=VDDQ
GND	VDDI=VDDQ

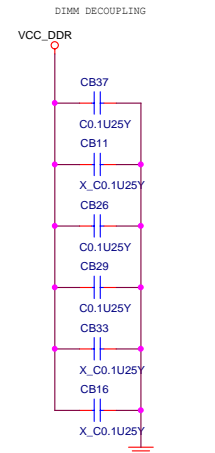
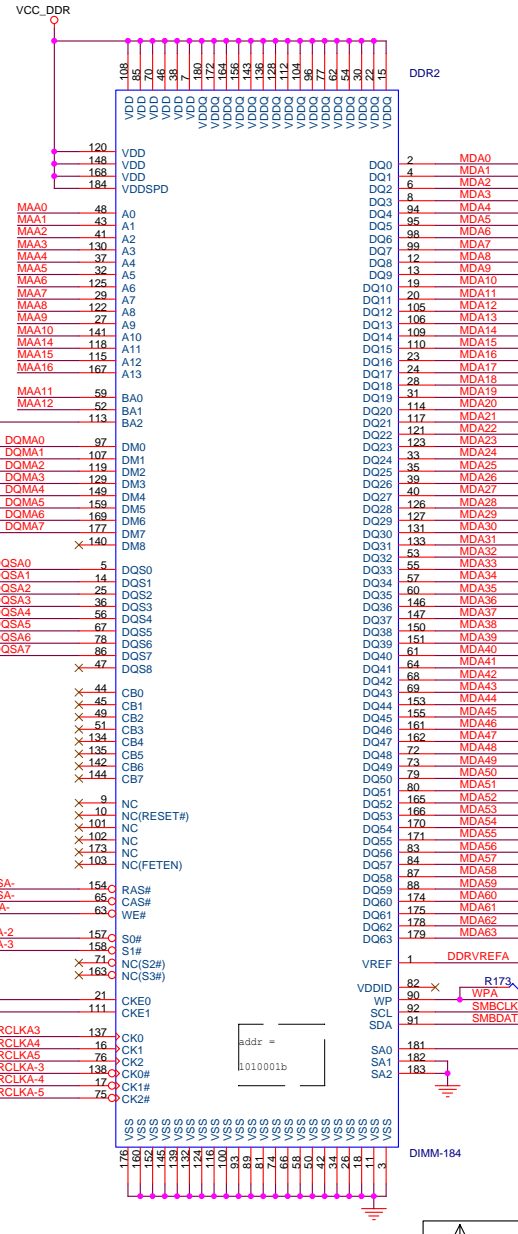
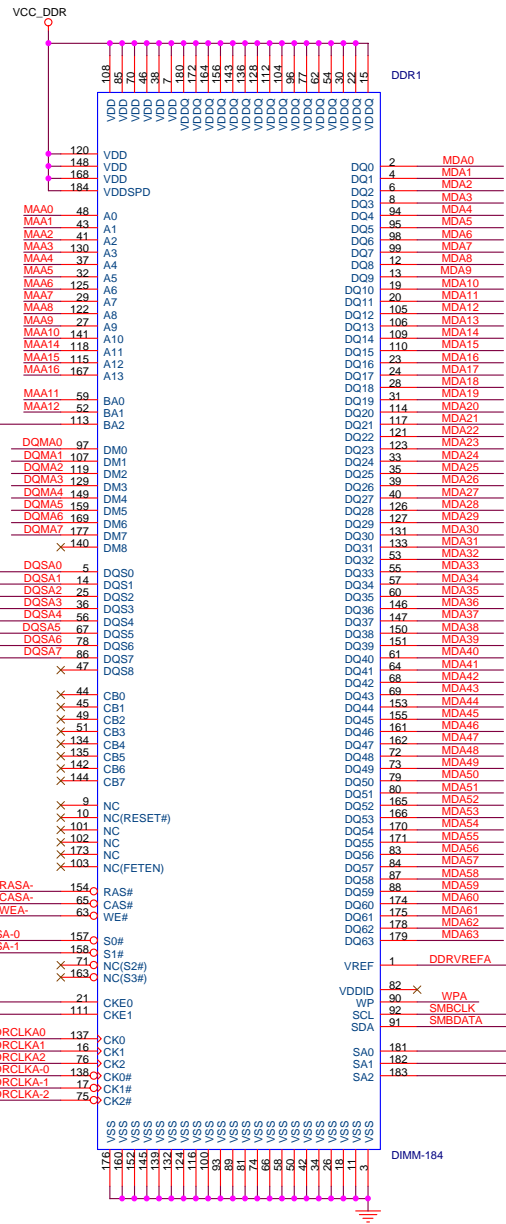
MEMORY MUX TABLE:

SDR	DDR
CS0	CS0
CS1	CS1
CS2	CS2
CS3	CS3
CS4	CS4
CS5	CS5
CSB0	DQS0
CSB1	DQS2
CSB2	DQS3
CSB3	DQS4
CSB4	DQS5
CSB5	DQS6
CSB6	DQS7
CSB7	DQS7

DDRREF GEN. & DECOUPLING



8,14 RASA- << RASA- 154
8,14 CASH- << CASH- 65
8,14 WEA- << WEA- 63
8,14 CSA-0 << CSA-0 157
8,14 CSA-1 << CSA-1 158
When ECC are enabled
8 CKEA0 << CKEA0 21
8 CKEA1 << CKEA1 111
Default
DDRCLKA0 137
DDRCLKA1 16
DDRCLKA2 76
DDRCLKA-0 138
DDRCLKA-1 17
DDRCLKA-2 75



25 DDRCLKB[0..5] << DDRCLKB[0..5]
25 DDRCLKB[0..5] << DDRCLKB[0..5]
9,15 MDB[0..63] << MDB[0..63]
9,15 MAB[14..16] << MAB[14..16]
9,15 MAB[0..12] << MAB[0..12]
9,15 DQMB[0..7] << DQMB[0..7]
9,15 DOSB[0..7] << DOSB[0..7]

NOTE:

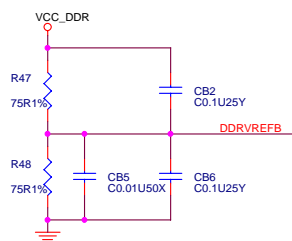
VDDID IS A TRAP ON THE DIMM
MODULE TO INDICATE:

VDDID	REQUIRED POWER
OPEN	VDD=VDDQ
GND	VDDI=VDDQ

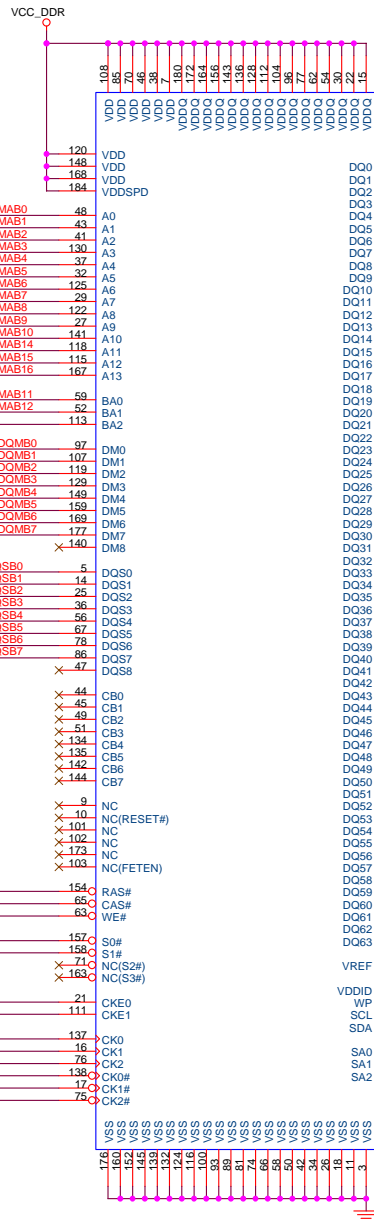
MEMORY MUX TABLE:

SDR	DDR
CS0	CS0
CS1	CS1
CS2	CS2
CS3	CS3
CS4	CS4
CS5	CS5
CSB0	DQS0
CSB1	DQS1
CSB2	DQS2
CSB3	DQS3
CSB4	DQS4
CSB5	DQS5
CSB6	DQS6
CSB7	DQS7

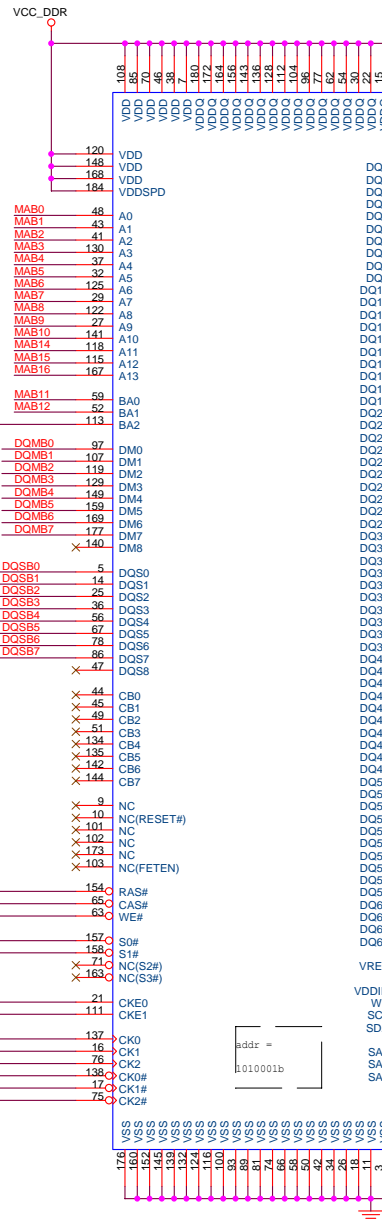
DDRREF GEN. & DECOUPLING



9,15 RASB << RASB-
9,15 CASB << CASB-
9,15 WEB << WEB-
9,15 CSB-0 << CSB-0
9,15 CSB-1 << CSB-1
9 CKEB0 << CKEB0
9 CKEB1 << CKEB1
DDRCLKB0 << CK0
DDRCLKB1 << CK1
DDRCLKB2 << CK2
DDRCLKB-0 << CK0#
DDRCLKB-1 << CK1#
DDRCLKB-2 << CK2#

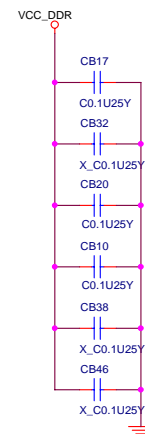


DQ0 2 MDB0
DQ1 4 MDB1
DQ2 6 MDB2
DQ3 8 MDB3
DQ4 94 MDB4
DQ5 95 MDB5
DQ6 98 MDB6
DQ7 12 MDB7
DQ8 12 MDB8
DQ9 13 MDB9
DQ10 19 MDB10
DQ11 20 MDB11
DQ12 105 MDB12
DQ13 106 MDB13
DQ14 109 MDB14
DQ15 110 MDB15
DQ16 23 MDB16
DQ17 24 MDB17
DQ18 28 MDB18
DQ19 31 MDB19
DQ20 114 MDB20
DQ21 117 MDB21
DQ22 121 MDB22
DQ23 123 MDB23
DQ24 33 MDB24
DQ25 35 MDB25
DQ26 39 MDB26
DQ27 40 MDB27
DQ28 126 MDB28
DQ29 127 MDB29
DQ30 131 MDB30
DQ31 133 MDB31
DQ32 53 MDB32
DQ33 55 MDB33
DQ34 57 MDB34
DQ35 60 MDB35
DQ36 146 MDB36
DQ37 147 MDB37
DQ38 150 MDB38
DQ39 151 MDB39
DQ40 61 MDB40
DQ41 64 MDB41
DQ42 68 MDB42
DQ43 69 MDB43
DQ44 153 MDB44
DQ45 155 MDB45
DQ46 161 MDB46
DQ47 162 MDB47
DQ48 72 MDB48
DQ49 73 MDB49
DQ50 79 MDB50
DQ51 80 MDB51
DQ52 165 MDB52
DQ53 166 MDB53
DQ54 170 MDB54
DQ55 171 MDB55
DQ56 83 MDB56
DQ57 84 MDB57
DQ58 87 MDB58
DQ59 88 MDB59
DQ60 174 MDB60
DQ61 175 MDB61
DQ62 178 MDB62
DQ63 179 MDB63
VREF 1 DDRREFB
VDDID 82 WPB
SCL 92 SMBCLK
SDA 91 SMBDATA
SA0 181 CK0
SA1 182 CK1
SA2 183 CK2



9,15 RASB << RASB-
9,15 CASB << CASB-
9,15 WEB << WEB-
9,15 CSB-2 << CSB-2
9,15 CSB-3 << CSB-3
9 CKEB2 << CKEB2
9 CKEB3 << CKEB3
DDRCLKB3 << CK0
DDRCLKB4 << CK1
DDRCLKB5 << CK2
DDRCLKB-3 << CK0#
DDRCLKB-4 << CK1#
DDRCLKB-5 << CK2#

DIMM DECOUPLING



VREF 1 DDRREFB
VDDID 82 WPB
SCL 92 SMBCLK
SDA 91 SMBDATA
SA0 181 CK0
SA1 182 CK1
SA2 183 CK2
addr = 010001b



MICRO-STAR

Title DDR3 & DDR4

Size Document Number MS-7114

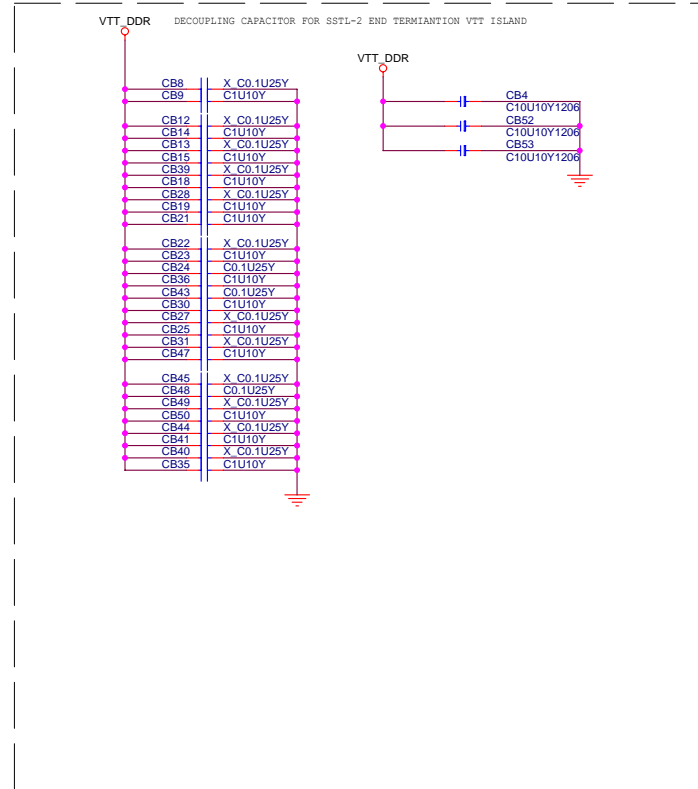
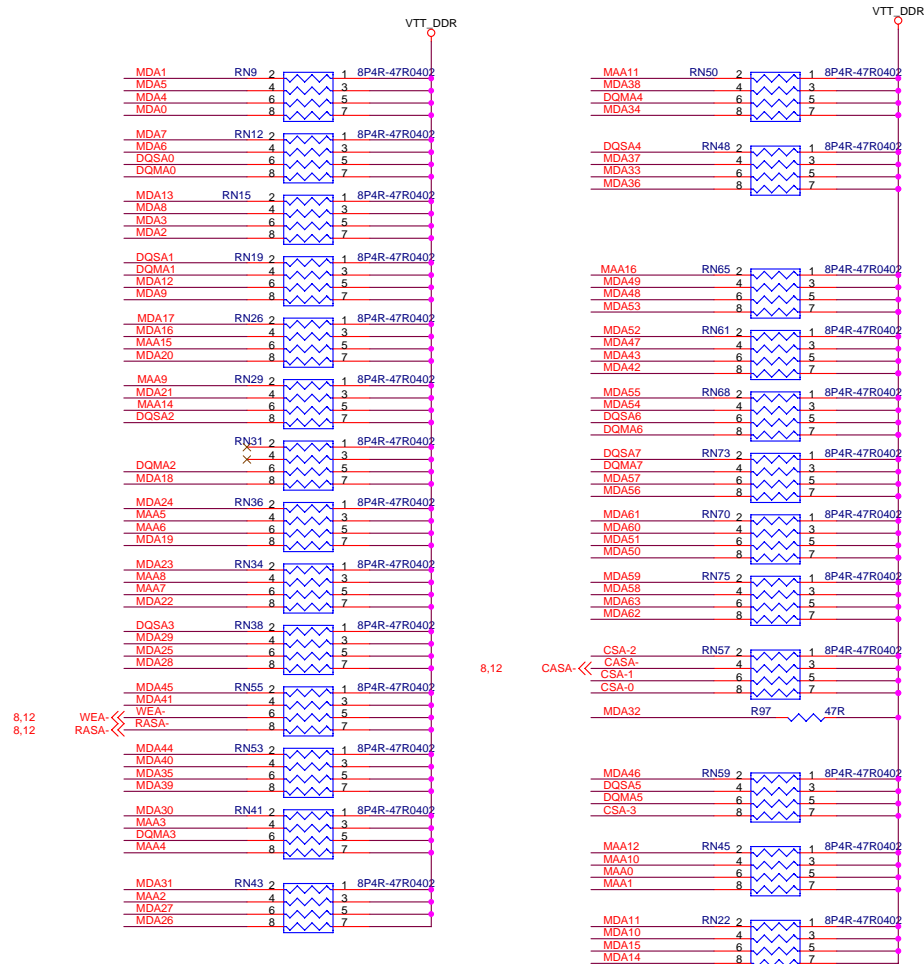
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DDR TERMINATOR

MDA0[0..63]	8,12
DQMA0[0..7]	8,12
DQSA0[0..7]	8,12
MAA14[14..16]	8,12
MAA0[0..12]	8,12
CSA[0..3]	8,12

SSTL-2 Termination Resistors

	SDR		DDR		
MD/DQM (/DQS)	LV-CMOS	0/10/-	SSTL-2	10	03
MA/Control	LV-CMOS	10	SSTL-2	0	03
CS	LV-CMOS	0	SSTL-2	0	47
EME	DD 3.3V		DD 2.5V		



DDR TERMINATOR

SSTL-2 Termination Resistors

MD/DQM (/DQS)	SDR	Re	DDR	Re	Re
MA/Control	LV-CMOS	0/10/-	SSTL-2	10	03
CS	LV-CMOS	0	SSTL-2	0	03
WE	BD 3.3V		SSTL-2	BD 2.5V	47

MDB[0..63]	<<MDB[0..63]	9,13
DQMB[0..7]	<<DQMB[0..7]	9,13
DQSB[0..7]	<<DQSB[0..7]	9,13
MAB[0..12]	<<MAB[0..12]	9,13
MAB[14..16]	<<MAB[14..16]	9,13
CSB[0..3]	<<CSB[0..3]	9,13

VTT_DDR

VTT_DDR

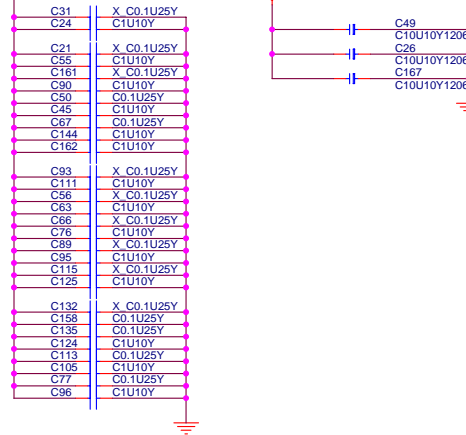
9,13 WEB- <<
9,13 RASB- <<

9,13 CASB- <<

VTT_DDR

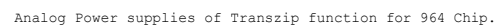
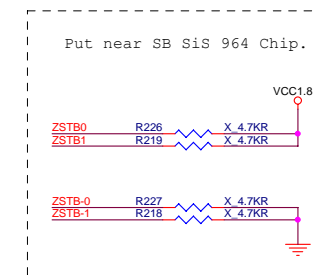
DECOUPLING CAPACITOR FOR SSTL-2 END TERMINATION VTT ISLAND

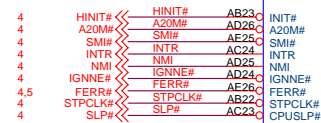
VTT_DDR



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Title	DDR TERMINATOR		
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CPU_S

APIC

LPC

MII

RTC

964-2

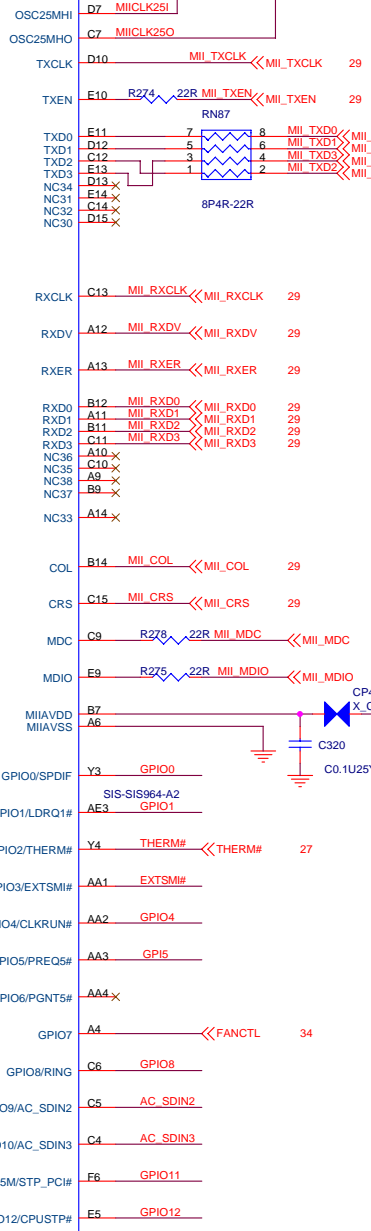
GPIO

AC97

ACPI / others

GPIO

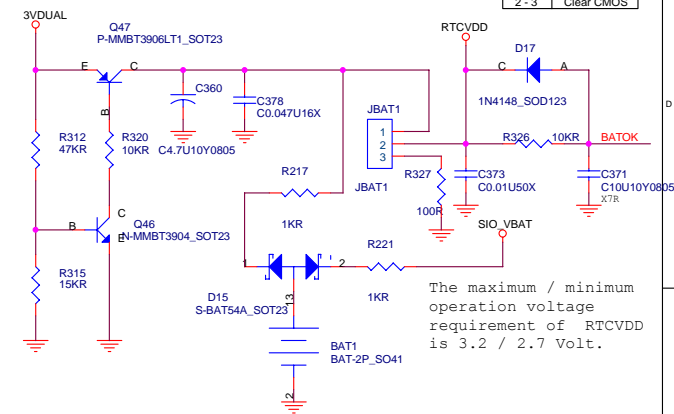
KBC



RTCVD should be more than 30 mils width

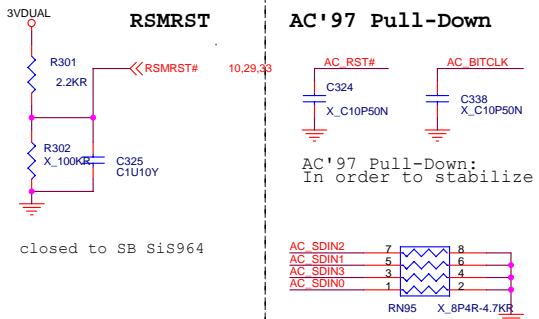
BATTERY BLOCK

CMOS CLEAR JUMPER	
JBAT1 Clear CMOS	
1-2	Normal
2-3	Clear CMOS



RSMRST

AC'97 Pull-Down

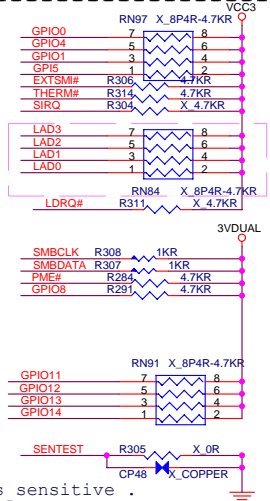


NEED NOT to place close to SB Sis964

GPIO 0~7 INTERNAL PULL UP
GPIO 9,10 INTERNAL PULL DOWN

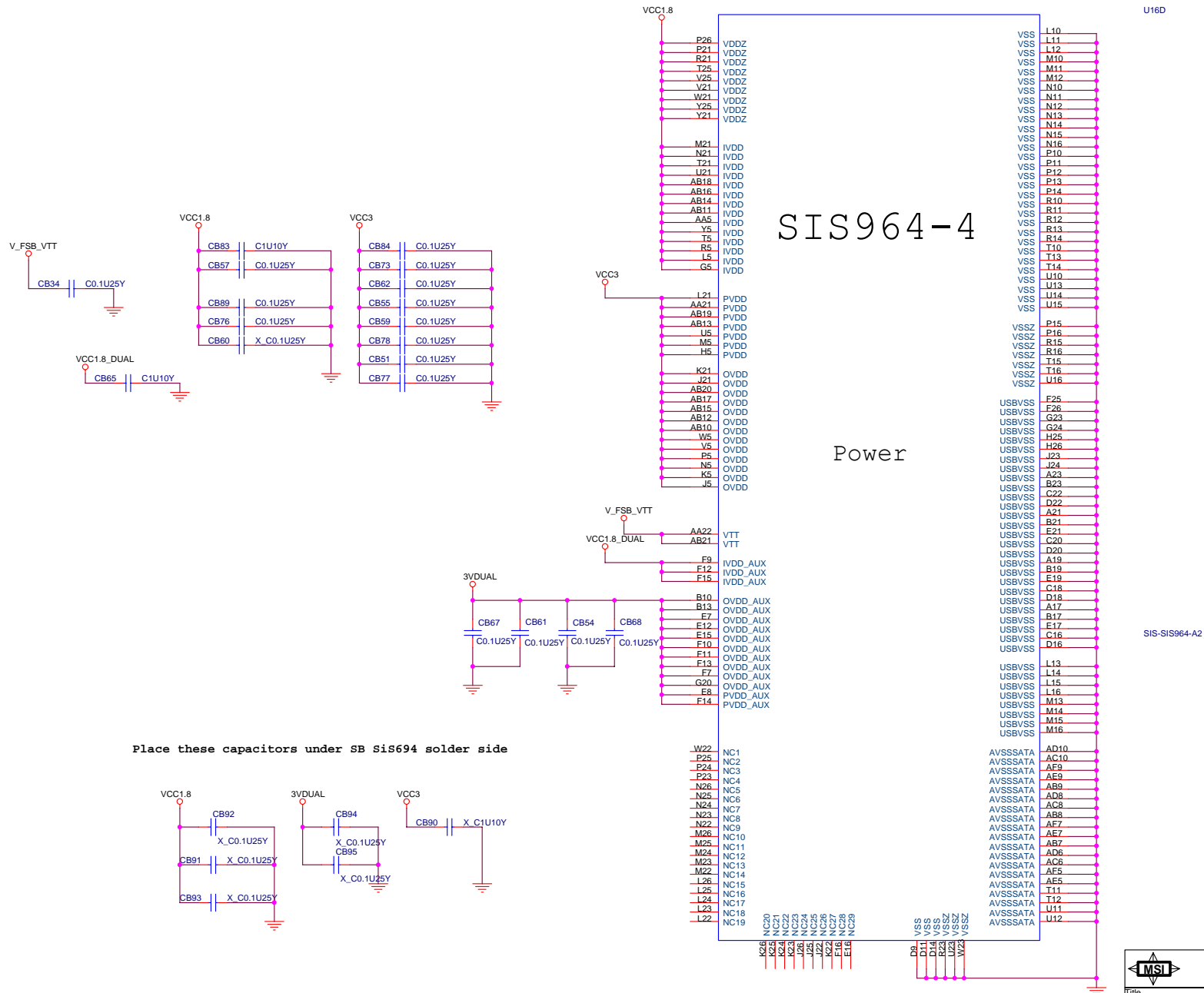
Register 72 ~ 73

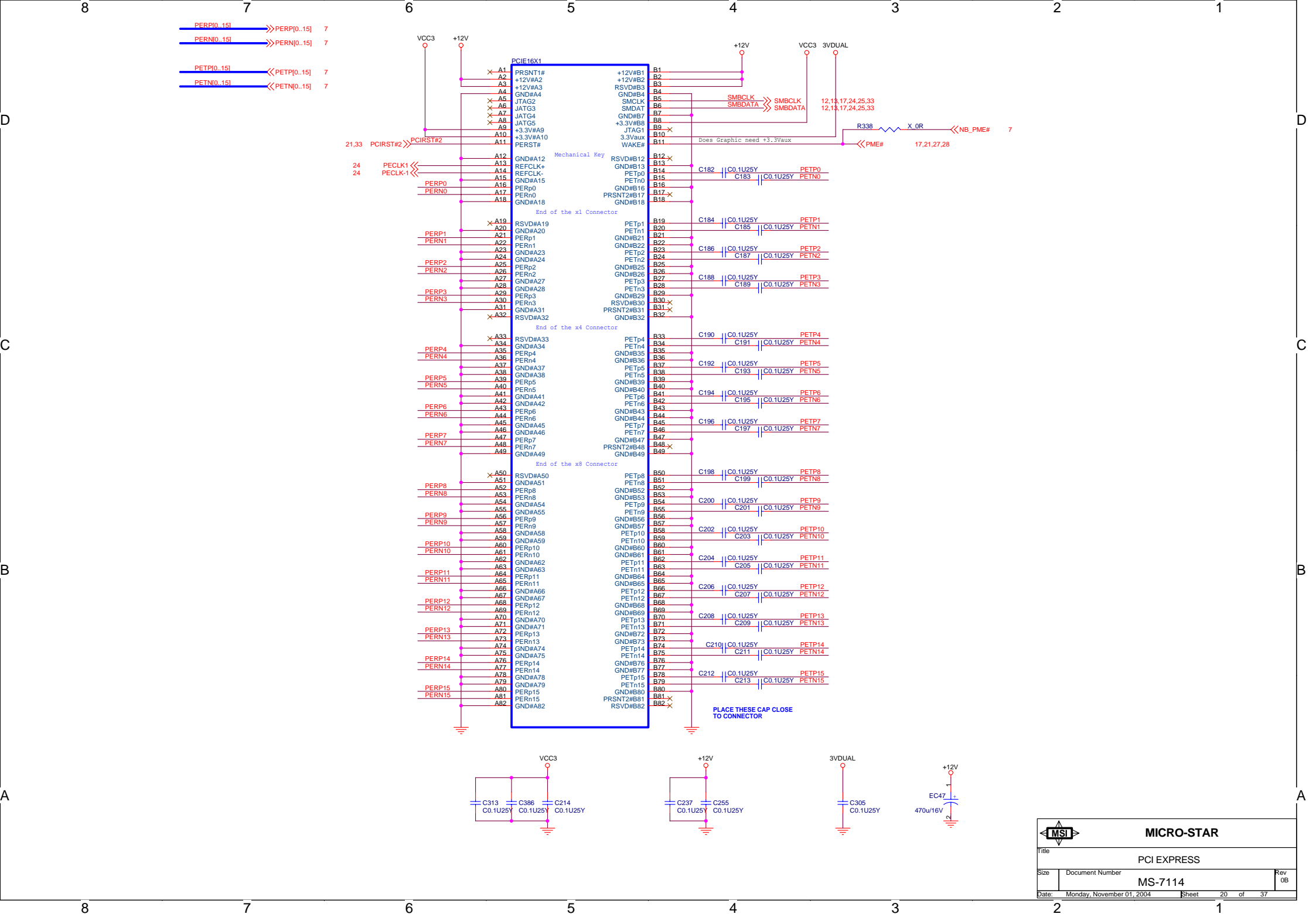
20040319
SiS garychen [garychen@sis.com] suggestion :
I think Pull-up resistors in LADs, LDREQ, and SRQ, are not necessary. However, I still recommend you to have these pads reserved in case of any problems in the future.



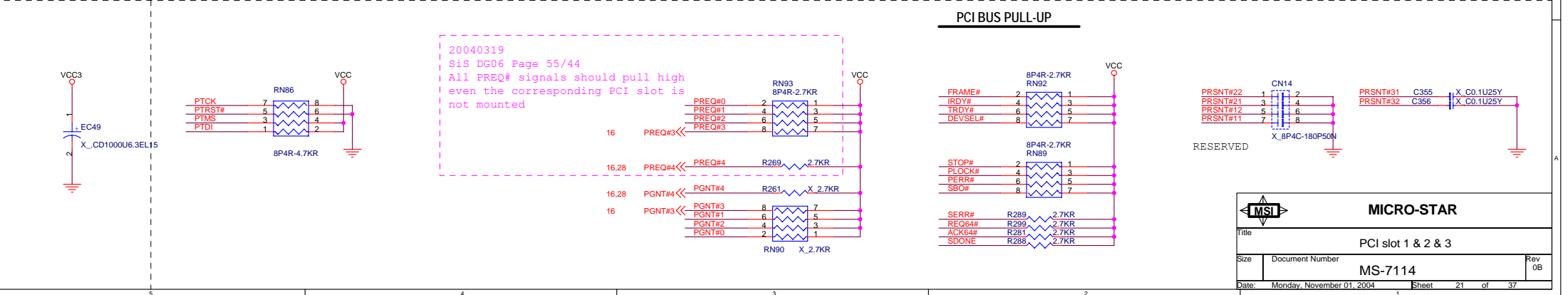
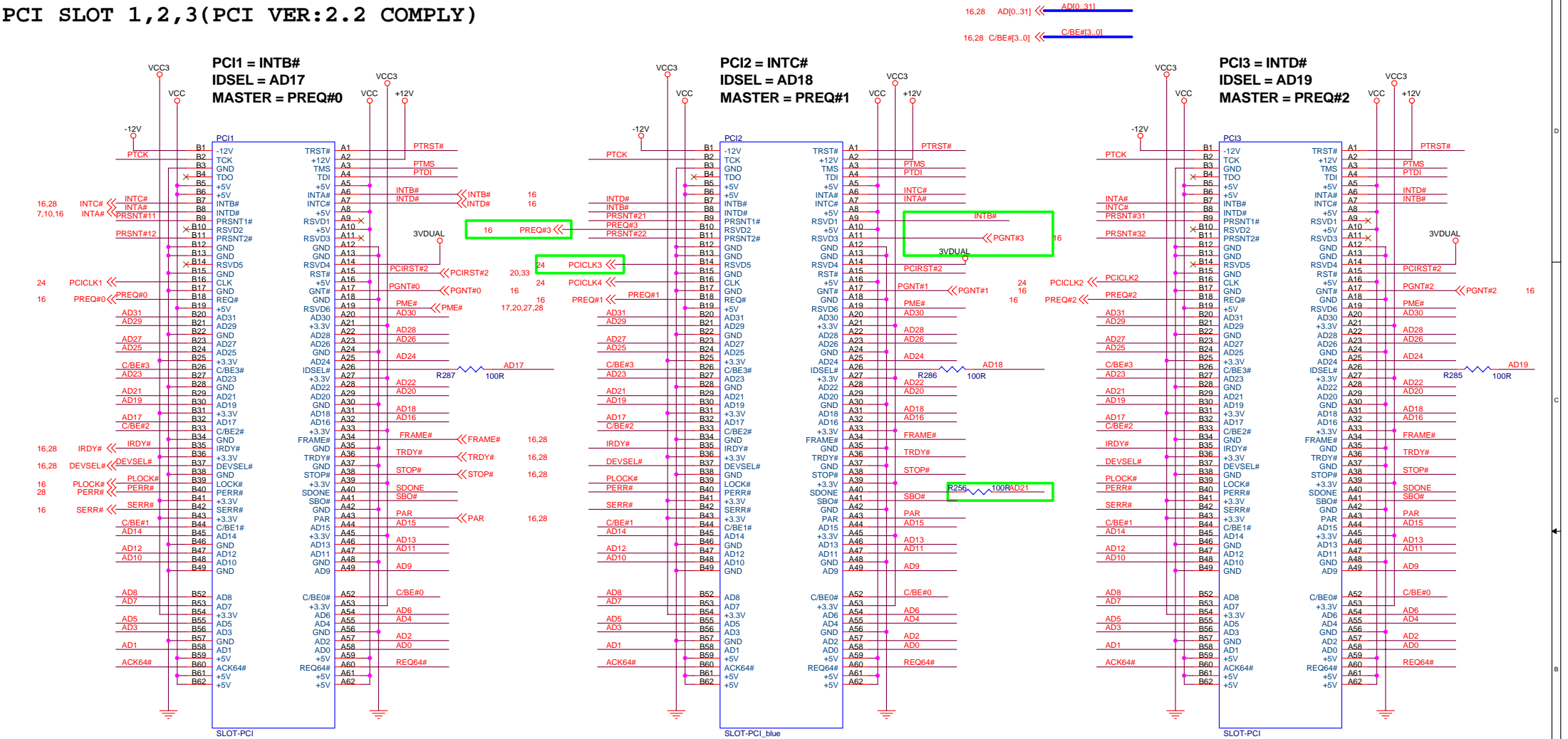
ENTEST pin is sensitive .
5 / 15

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Title: SIS964(MISC.)		
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PCI SLOT 1,2,3(PCI VER:2.2 COMPLY)



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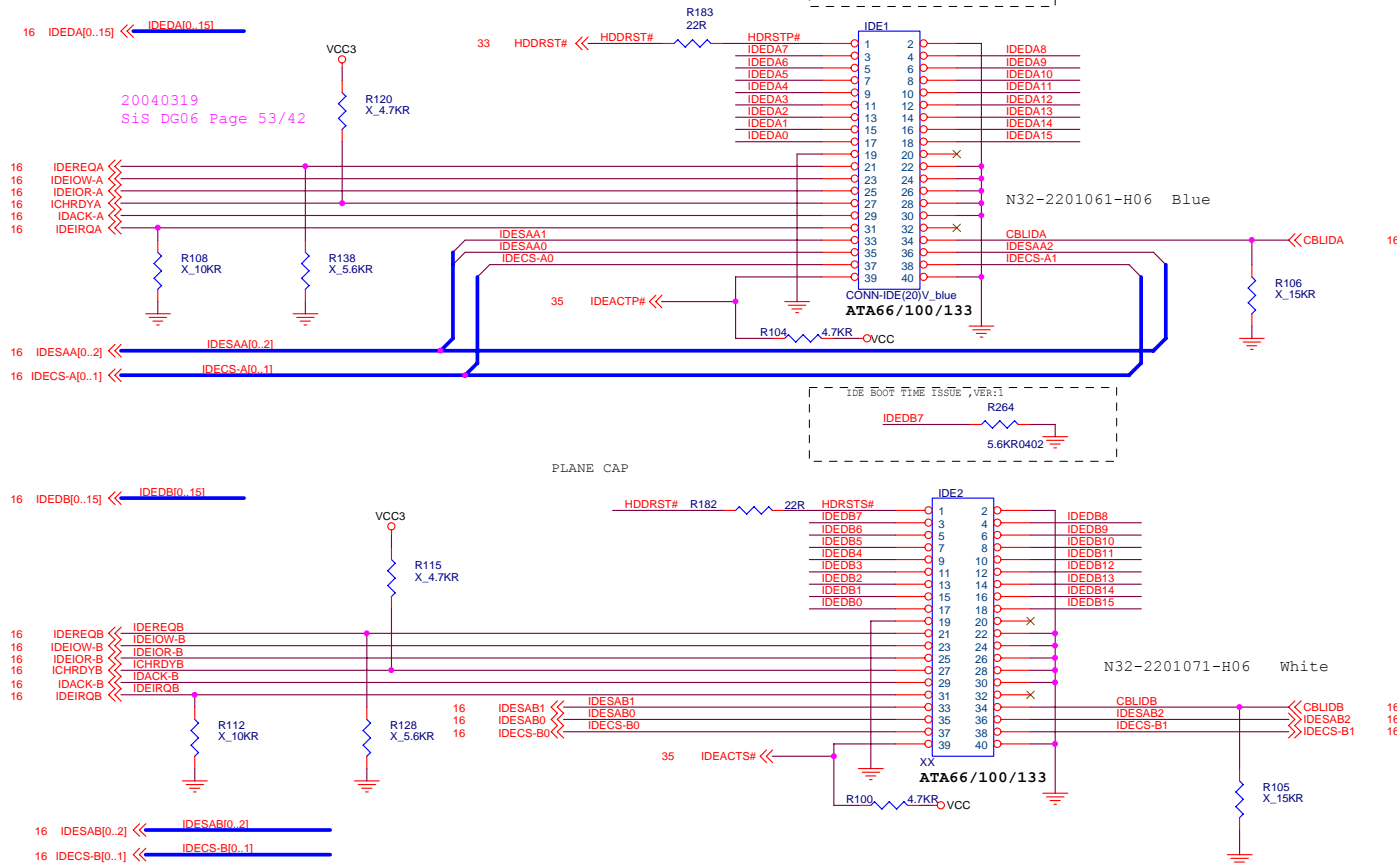
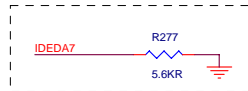
Sheet 21 of 37

Rev 08

IDE1 & IDE2

20040319
Sis AP note : A964008

IDE BOOT TIME ISSUE ,VER:1



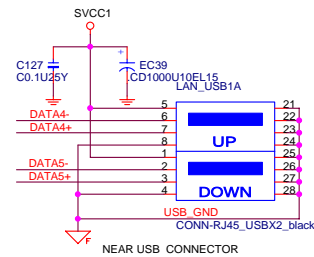
MICRO-STAR

Title			
IDE-ATA			
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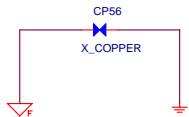
```

18      DATA4+ <<< DATA4+
18      DATA4+ <<< DATA4+
18      DATA5+ <<< DATA5+
18      DATA5+ <<< DATA5+

```



N58-20F0081-A11

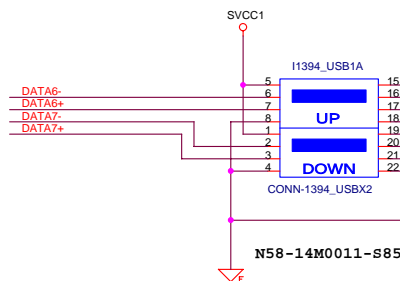


22 / 7.5 / 7.5 / 7.5 / 22 / 7.5 / 7.5 / 7.5 / 22

NEAR USB CONNECTOR

22 / 7.5 / 7.5 / 7.5 / 22 / 7.5 / 7.5 / 7.5 / 22

18	DATA6+ <<	DATA6+
18	DATA6- <<	DATA6-
18	DATA7+ <<	DATA7+
18	DATA7- <<	DATA7-



NEAR USB CONNECTOR

22 / 7.5 / 7.5 / 7.5 / 22 / 7.5 / 7.5 / 7.5 / 22

NEAR USB CONNECTOR
NEAR USB CONNECTOR

22 / 7.5 / 7.5 / 7.5 / 22 / 7.5 / 7.5 / 7.5 / 22

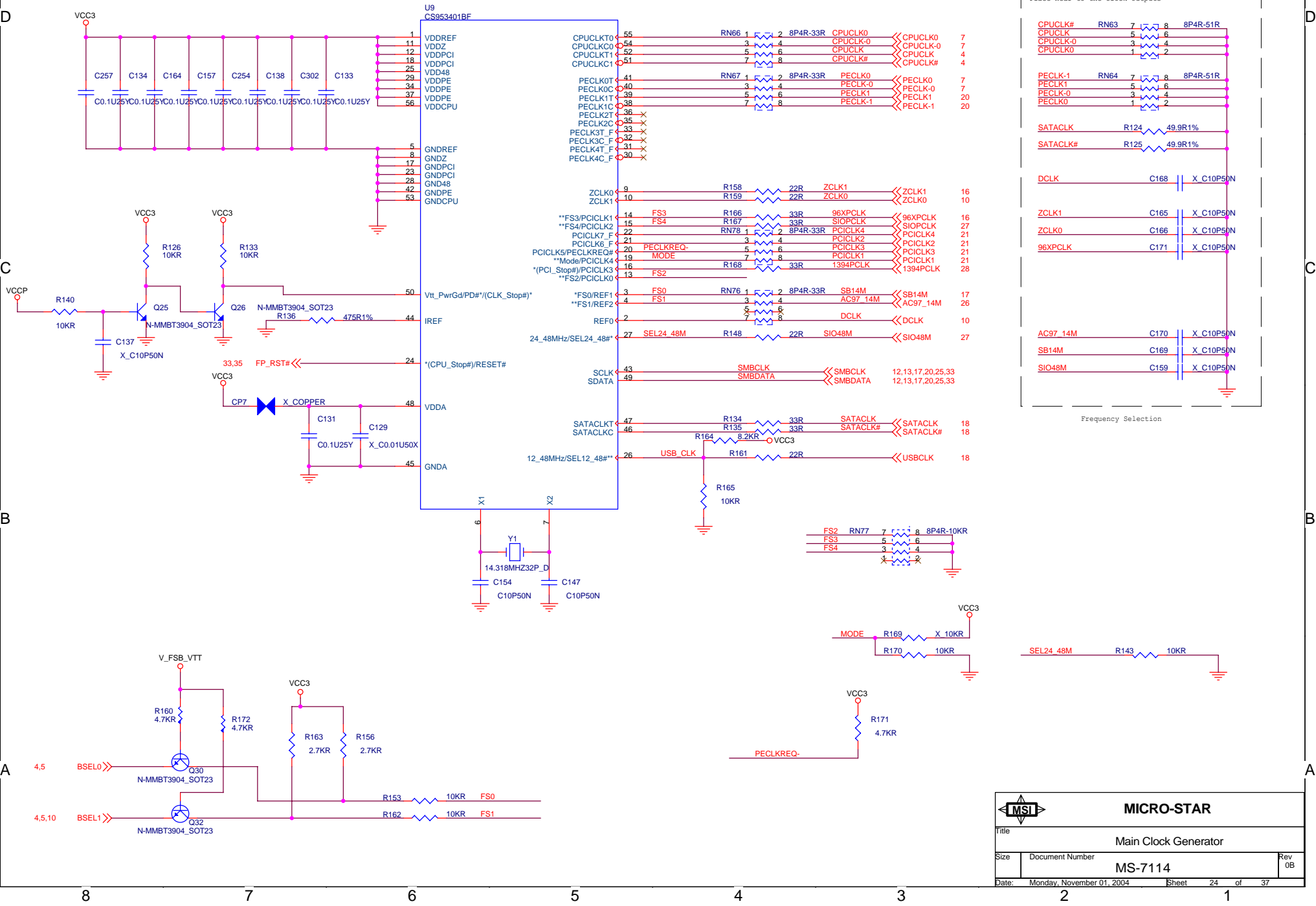


Size	Document Number
	MS-7114

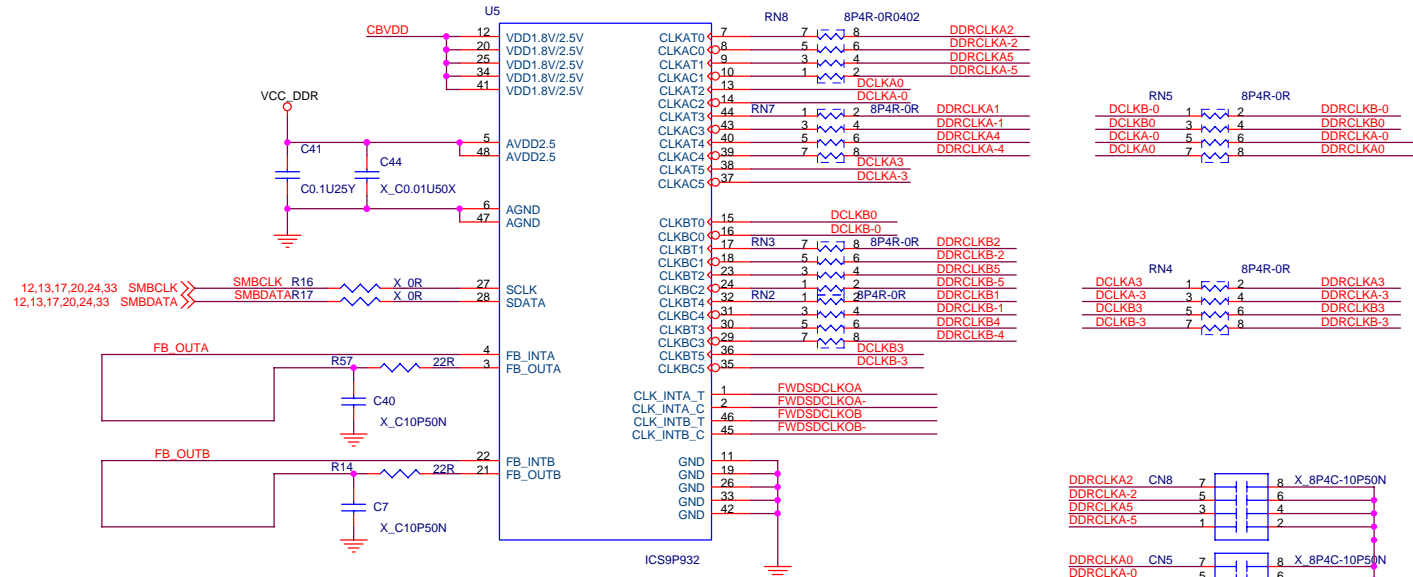
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Main Clock Generator

OPTIONS
1. ICS953401



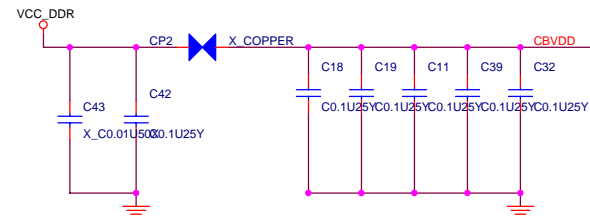
Clock Buffer (DDR)

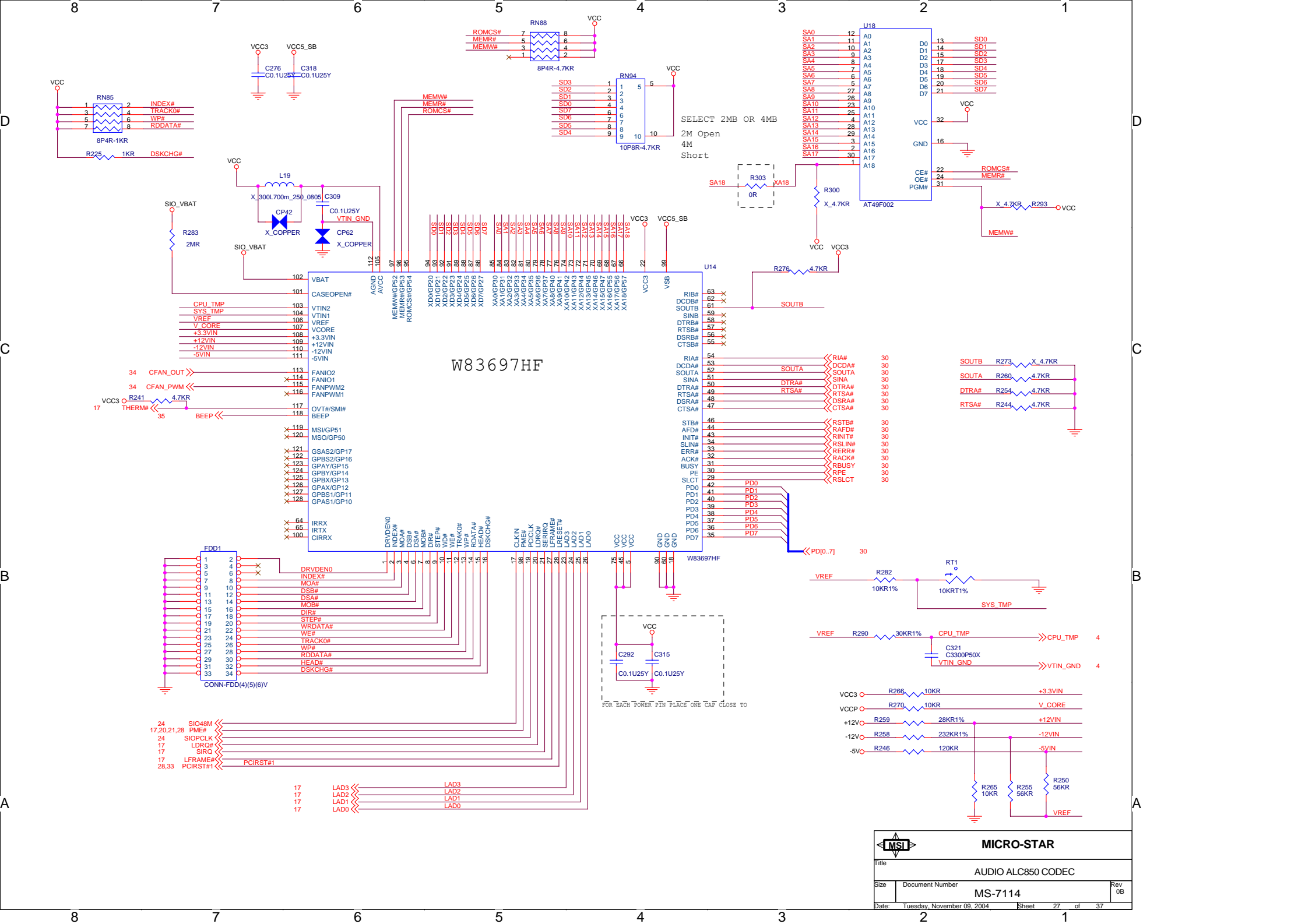


FWSDCLKOA << FWSDCLKOA 8
FWSDCLKOA- << FWSDCLKOA- 8
FWSDCLKOB << FWSDCLKOB 8
FWSDCLKOB- << FWSDCLKOB- 8

DDRCLKB[0..5] << DDRCLKB[0..5] 13
DDRCLKB-[0..5] << DDRCLKB-[0..5] 13
DDRCLKA[0..5] << DDRCLKA[0..5] 12
DDRCLKA-[0..5] << DDRCLKA-[0..5] 12

DDRVREF GEN. & DECOUPLING





IEEE-1394

The schematic diagram illustrates the power supply section of the IEEE-1394 interface. It features a 12V input connected to a diode bridge (D18, S-MBR340) and a filter capacitor (C372). The output is connected to a series of capacitors (C374, C1000P50X) and a diode (D18). The circuit then branches into three parallel paths, each with a diode bridge and filter capacitor (CP41, CP24, CP26). The output of these paths is connected to a series of capacitors (C295, C304, C306, C271, C267, C269, C266) and a diode (D18). The final output is connected to a series of capacitors (C316, C298, C307, C303, C308, C317, C314, C282) and a diode (D18).

FS5 F-MINISMDM150/24

BUS_PWR 1394_VCC2

TPB1AS1

R236 54.9R1% R237 54.9R1%

C293 C0.33U16Y

R233 4.99KR1% C279 C270P50N

R229 54.9R1% R234 54.9R1%

TPA1+ TPA1- TPA1 TPA1-

(T/S/S=7/10/10)

Place close to pin 97
(Less than 500 mils)

J1394_1

KEY GND POWER GND

TPB1+ TPB+ TPB- TPB-

GND GND GND

TPA+ TPA TPA

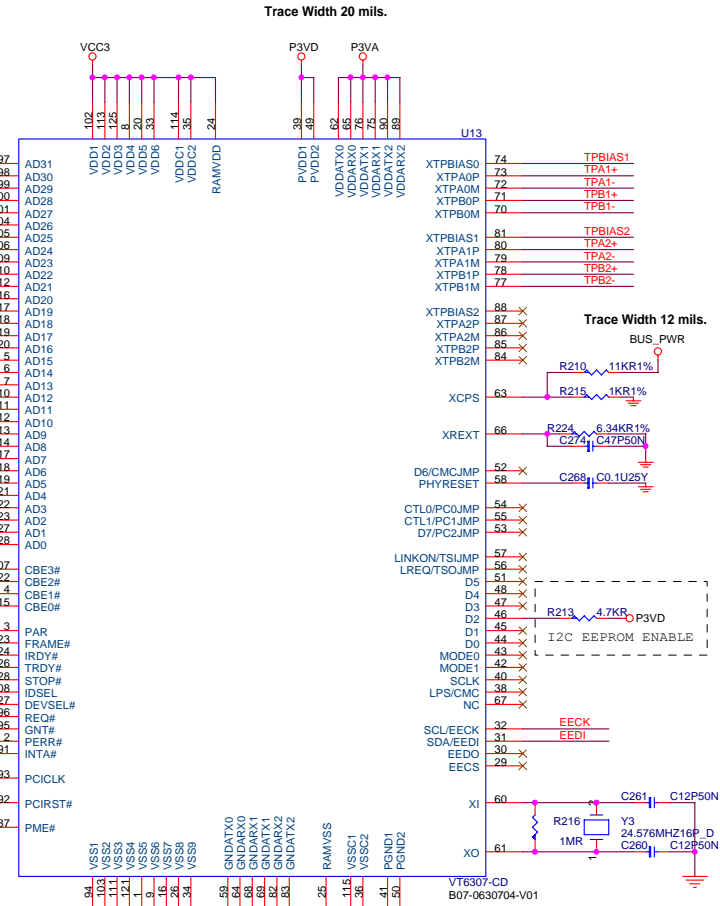
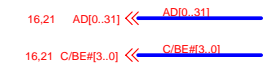
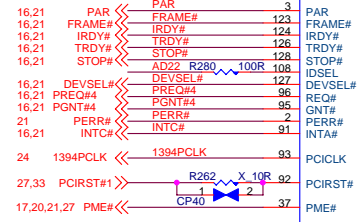
BH2X5(9)USB_black

1394_VCC2 TPA1+ TPA1- TPA1 TPA1-

CB85 C0.1U25Y

Place close to pin 111
(Less than 500 mils)

N58-14M0011-S85
Change to STARCONN



```
IDSEL AD22
MASTER = PREQ#4
INTD#
```

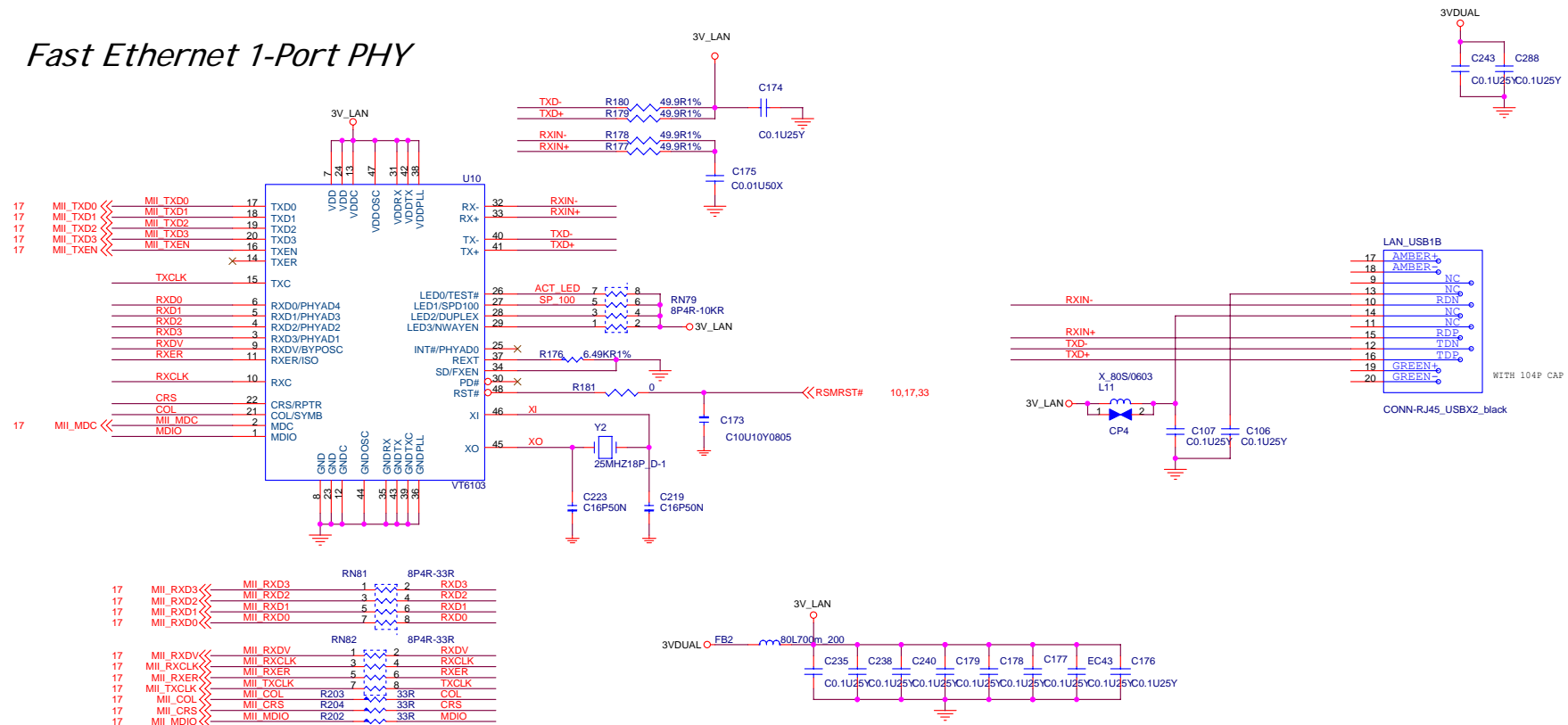


MICRO-STAR

Title 1394 - VIA VT-6307

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Fast Ethernet 1-Port PHY



MICRO-STAR

Title	LAN
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Size	Document Number
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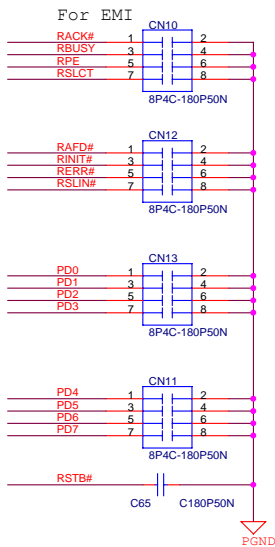
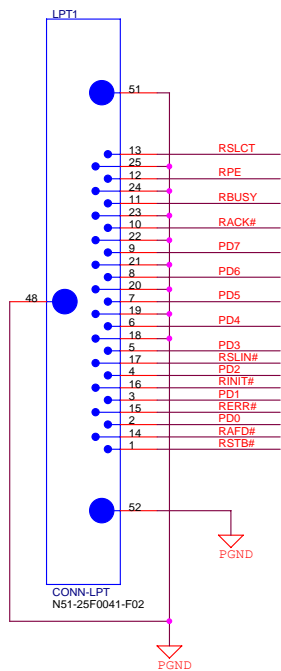
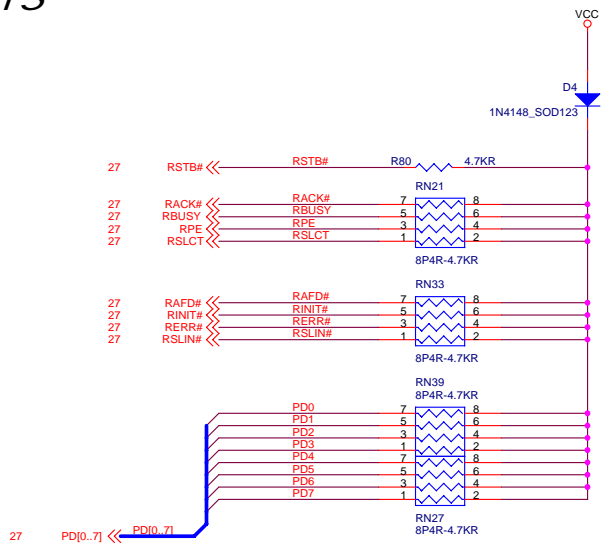
MS-7114

ev
0B

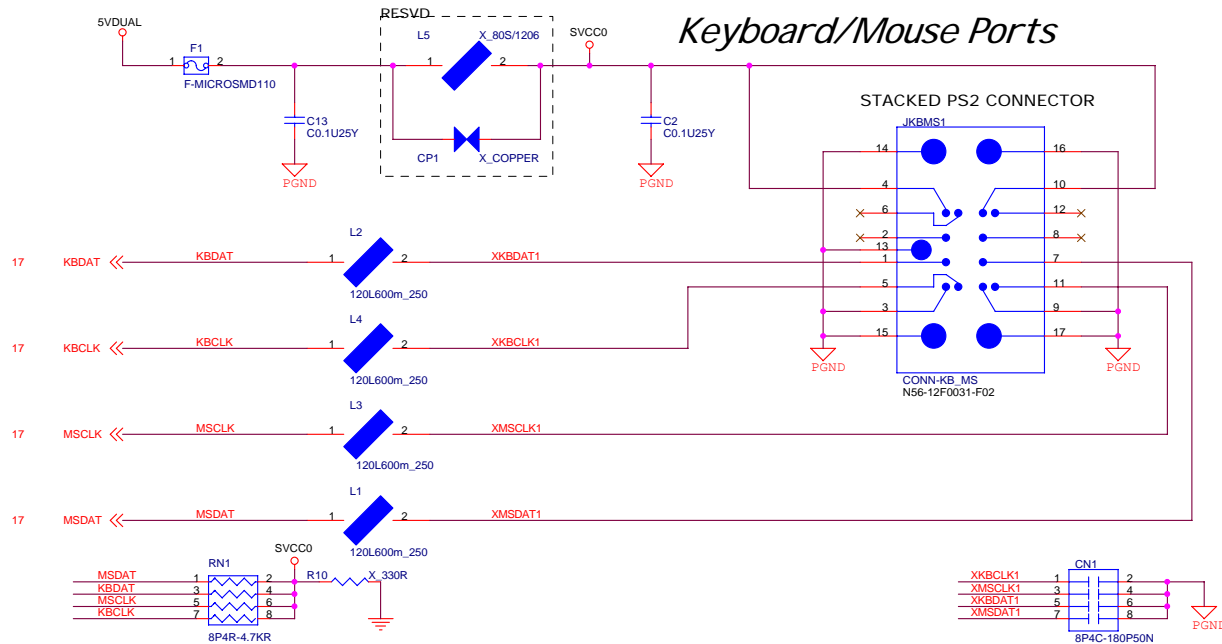
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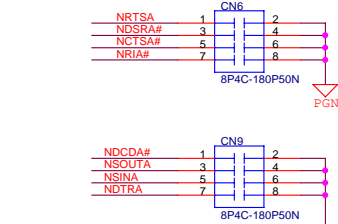
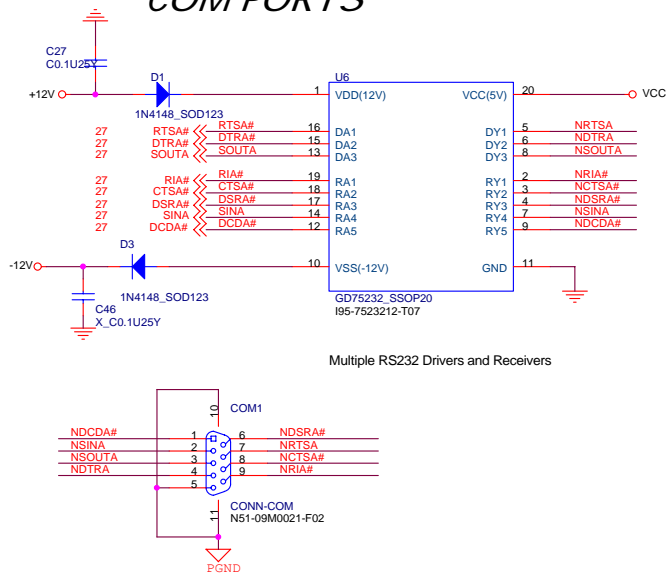
LPT PORTS



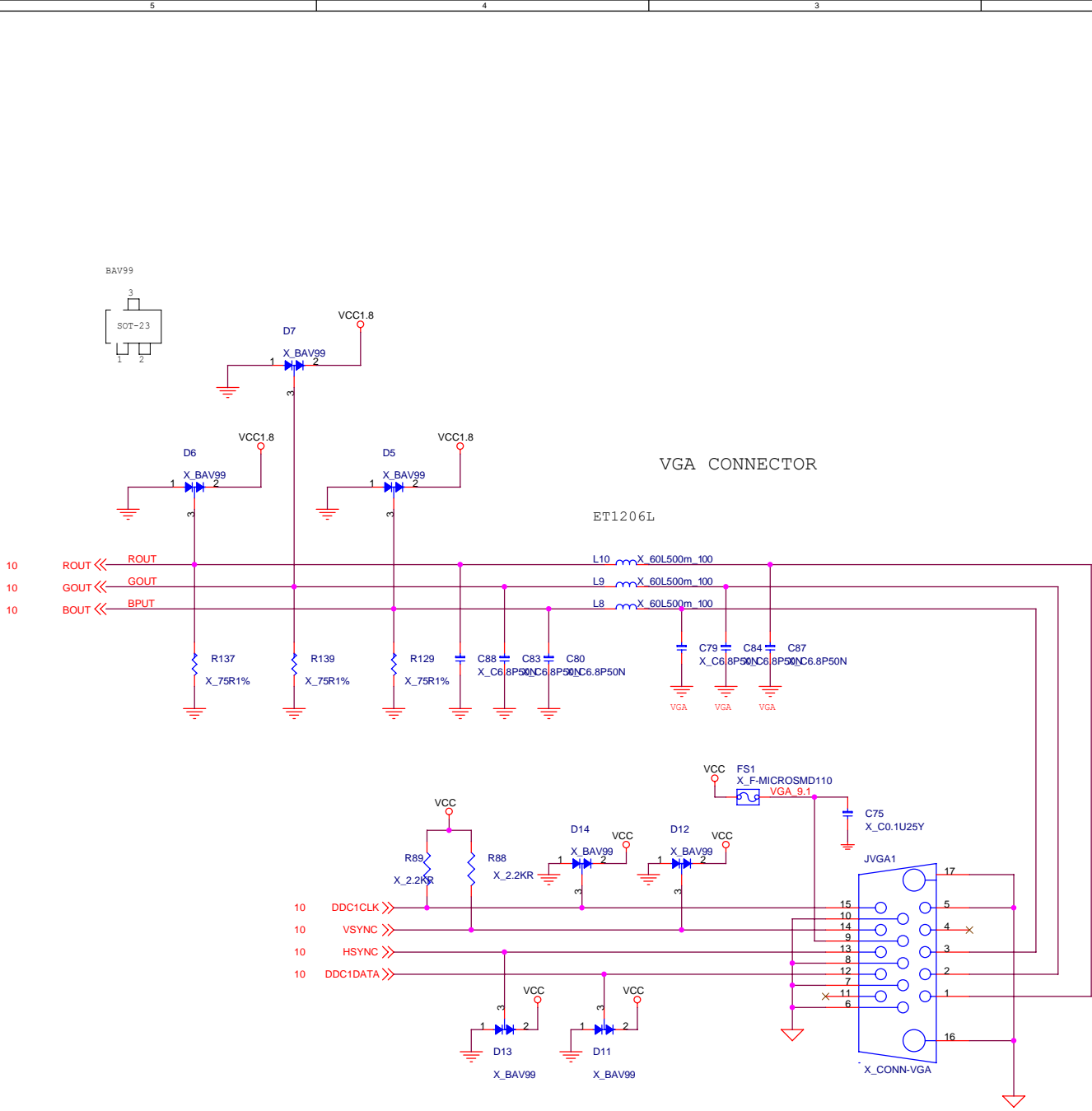
Keyboard/Mouse Ports



COM PORTS



Title LPT/COM PORT	
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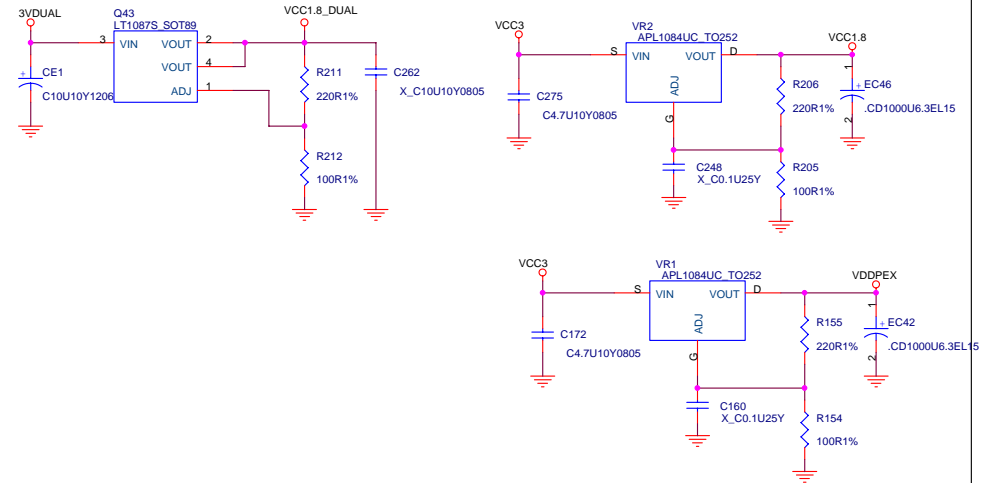
```
TDP = 115 W
VR_TDC = 101 A
Icc(max) = 119 A
Tejas Tcase = [P x 0.213] + 43.3
Prescott Tcase = [P x 0.25] +
43.3
```


ACPI Controller

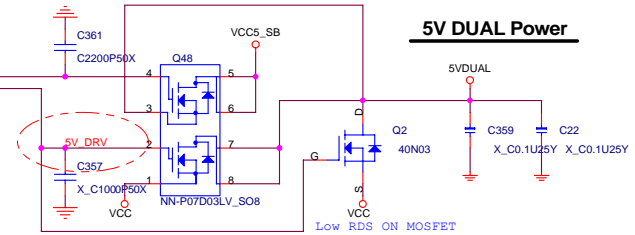
IC15 300mA
PCI 375+20+20= 415mA
VCC3_SB 715mA

Power	S0	S3	S5
VCC3_SB	Main	Standby	Standby
VCC5_STR	Main	Standby	0V
MEM_STR	Main	Standby	0V

1.8V STAND BY POWER

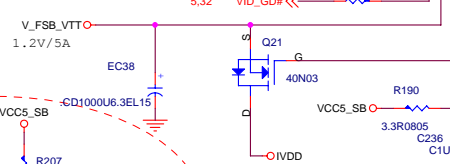


5V DUAL Power



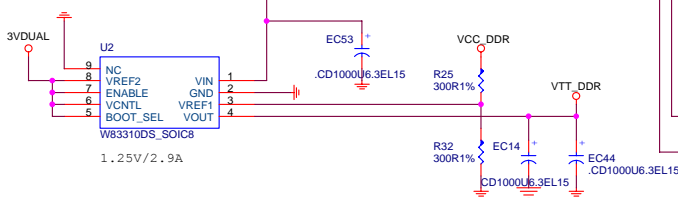
VCC_VID / VID_GOOD

Place MOSFET near CPU



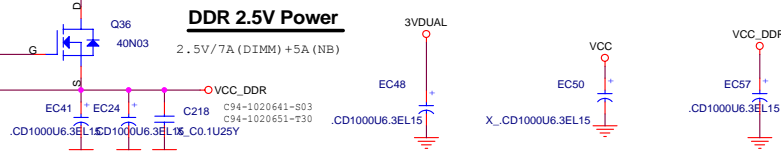
DDR VTT Power

1.25V/2.1A



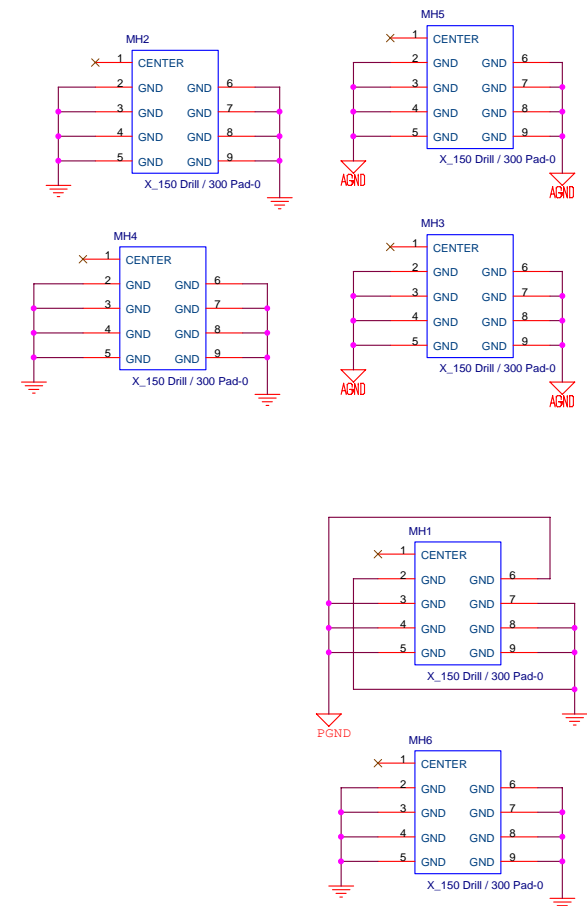
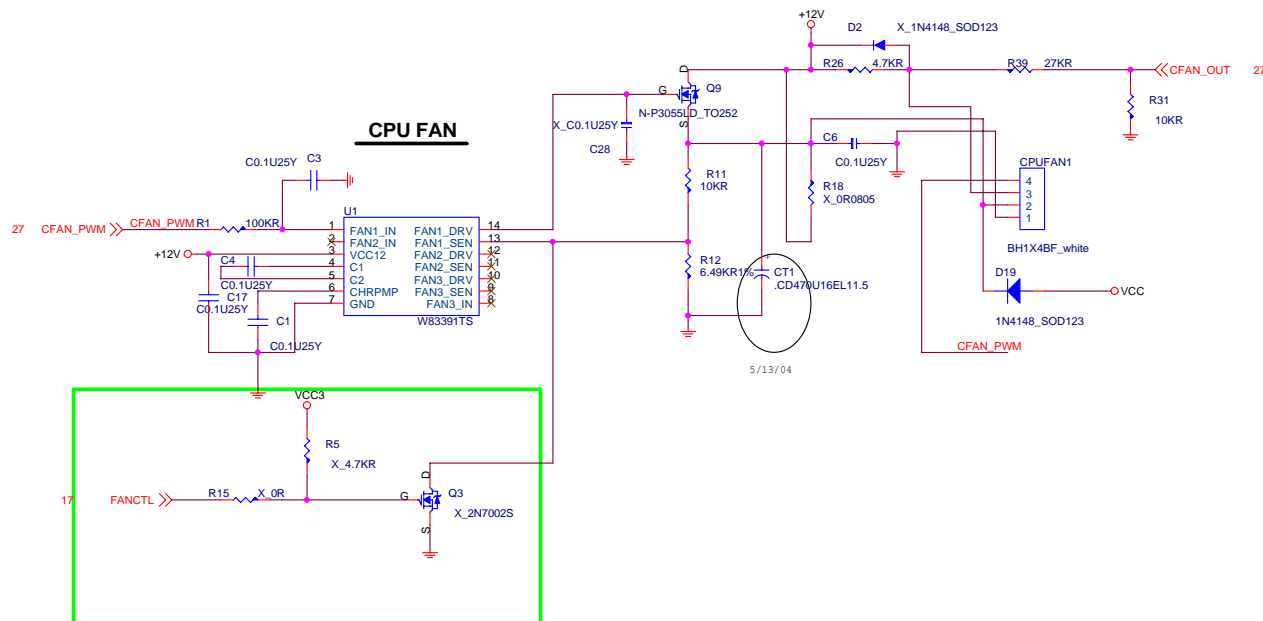
DDR 2.5V Power

2.5V/7A (DIMM) +5A (NB)

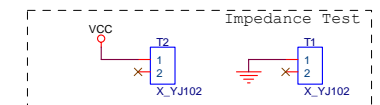
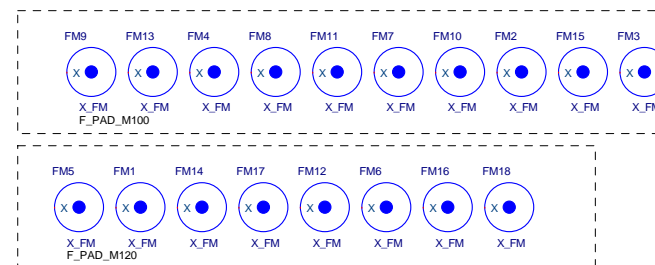
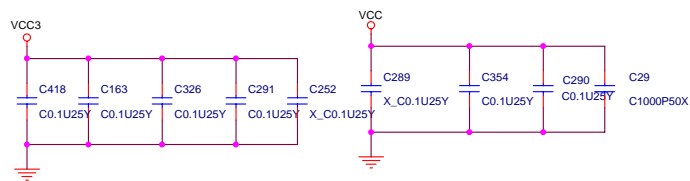


MSI MICRO-STAR			
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ACPI Controller MS7			
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ATX VIA-Hole * 9



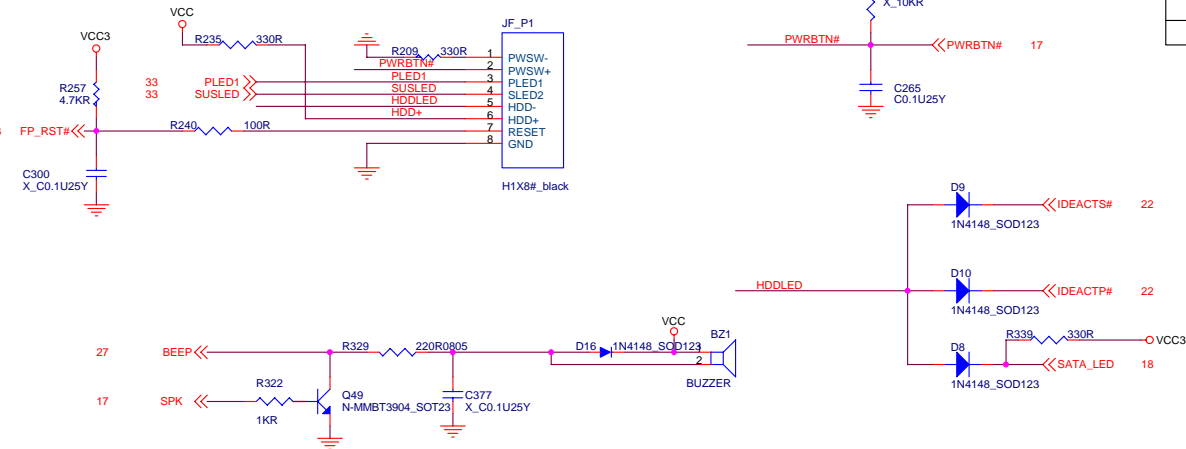
BULK / Decoupling



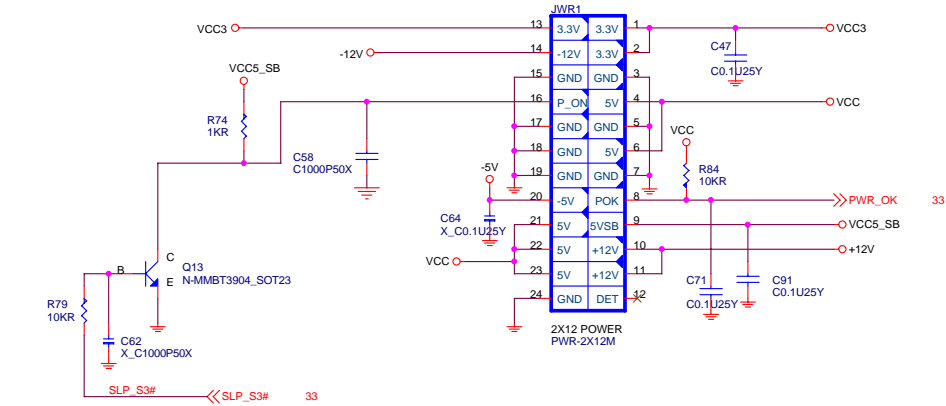
		MICRO-STAR	
		Title FAN	
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FRONT PANEL

For MSI / Front Panel



ATX Connector



PCB1



P00-071140B-E48

VBAT1-1



BAT-BCR2032P
D06-0100101-P01

U8_HS

MSI
DDR

NB-HEATSINK
E31-0401580-E25

U16_HS

MSI
DDR

X_SB-HEATSINK
E31-0400890-E25

U18_X




SST39SF040-70-4C-NH



MICRO-STAR

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Title HISTORY			
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